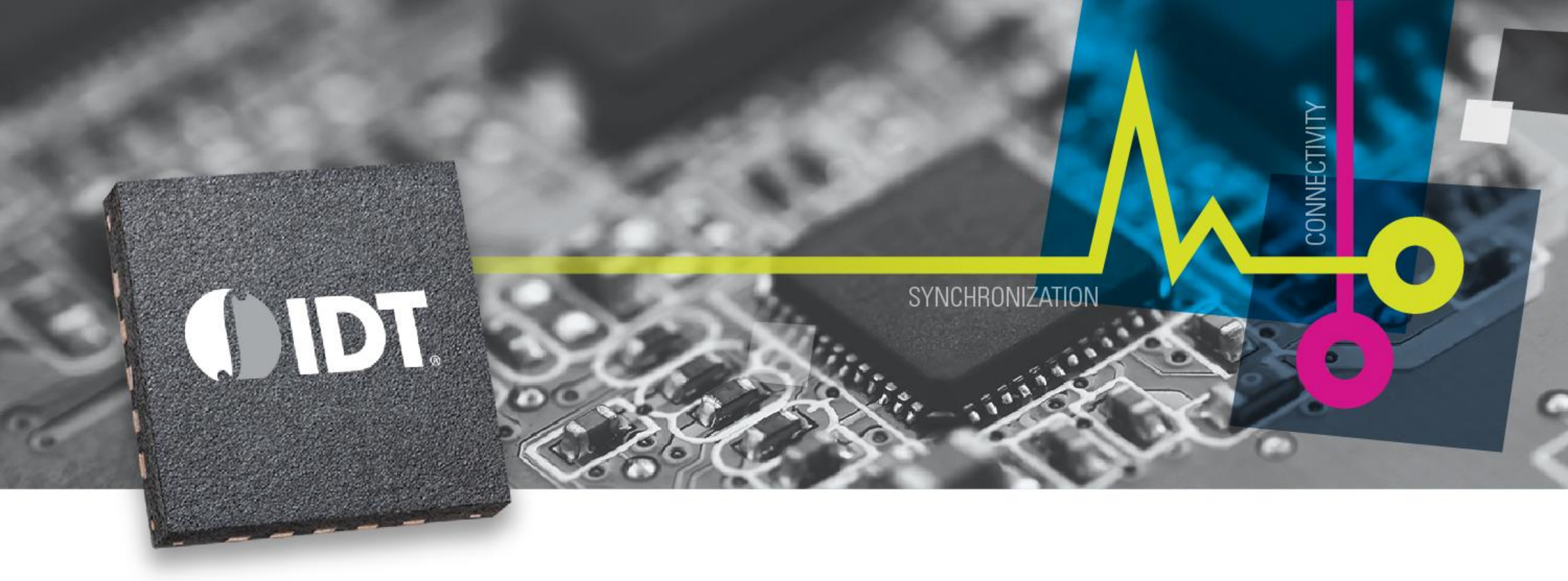

Tutorial:
Quartz Crystal Oscillators & Phase-Locked Loops

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Dominik Schneuwly (Oscilloquartz)

June 18th, 2018

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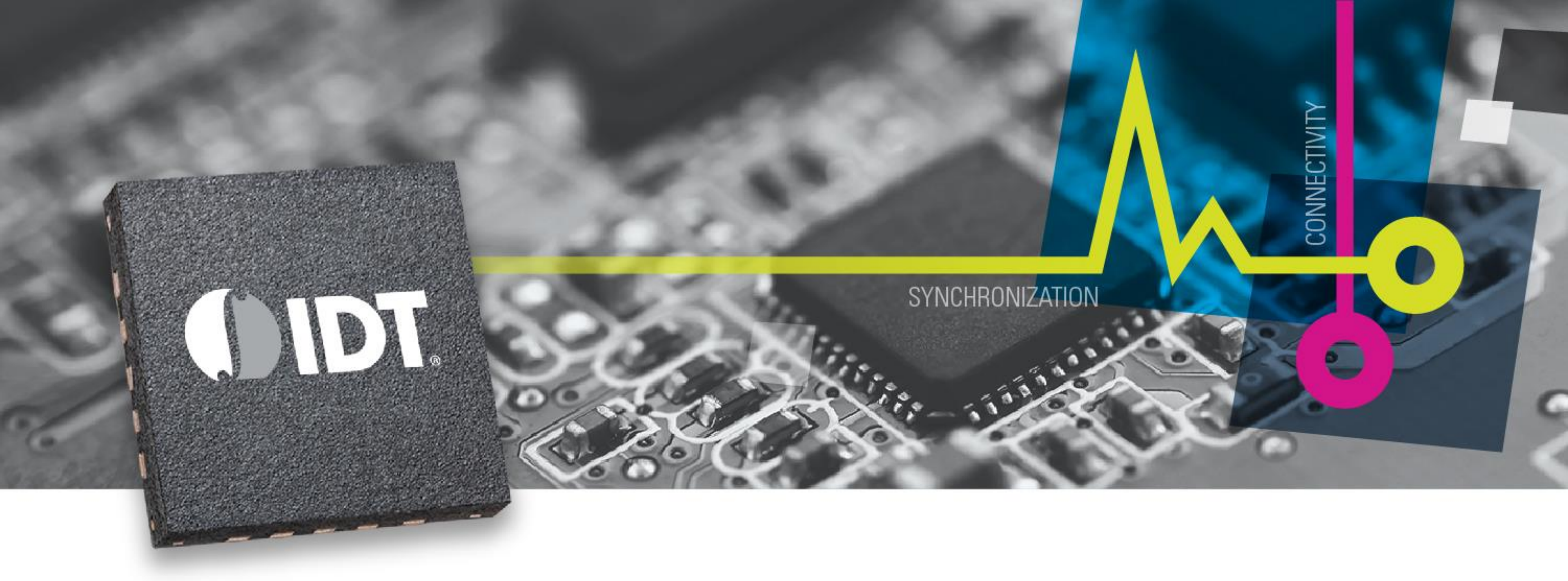
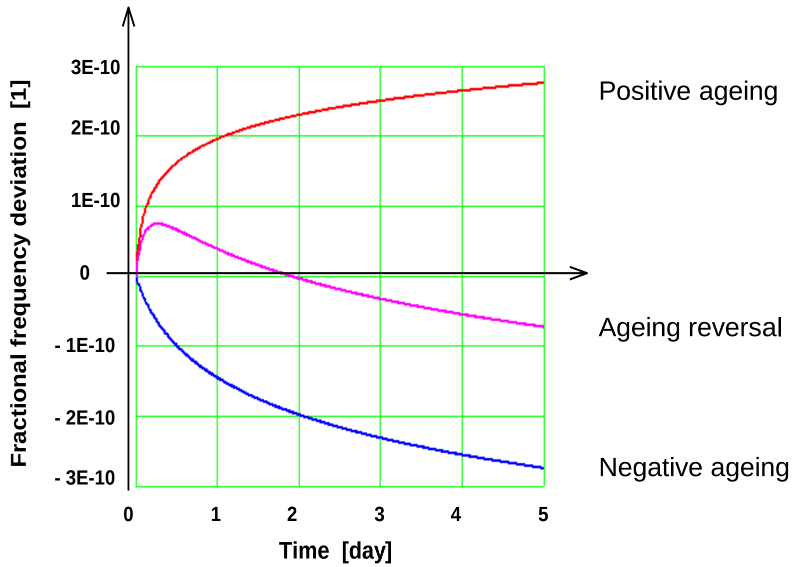


1. Quartz Crystal Oscillator (XO) Refresher

Frequency Drift Due to Ageing



Frequency vs. Temperature

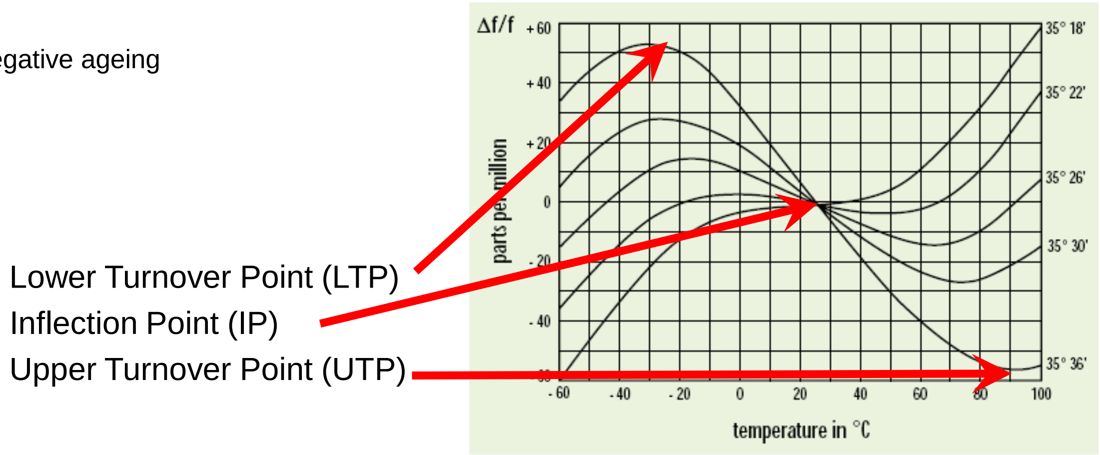
SC-cut:

Θ = 34°

Φ = 22°

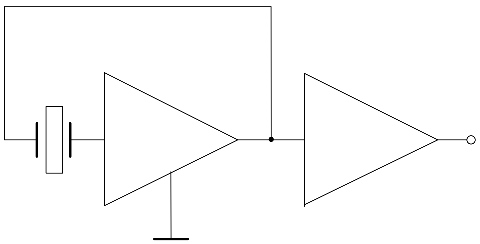
Δf/f as a function of temperature

(parameter: ΔΘ = deviation from reference angle)

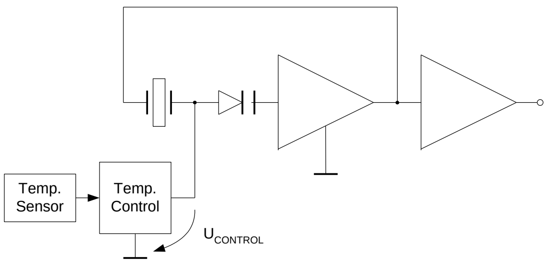


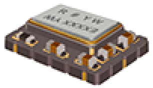
XO Categories rel. Temp. Control

- XO, (Uncompensated) Crystal Oscillator:
  - LTP centered in the operation temperature range
  - > 1E-7 / °C



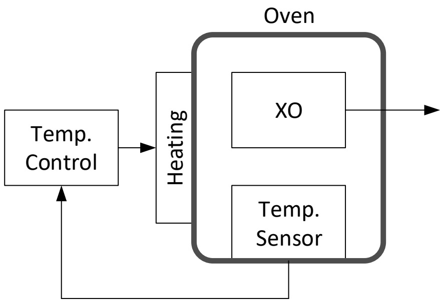
- TCXO, Temperature Compensated XO:
  - Resonance frequency is modified by a varactor diode so as to compensate temperature sensitivity
  - 5E-8 to 5E-7 over [-55°C to 85°C]

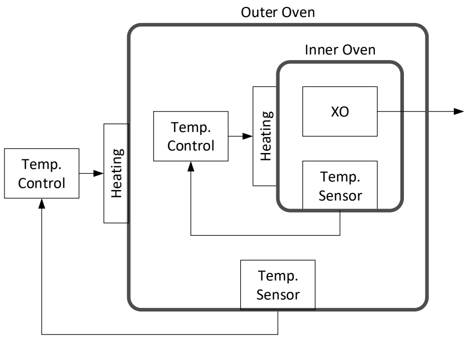


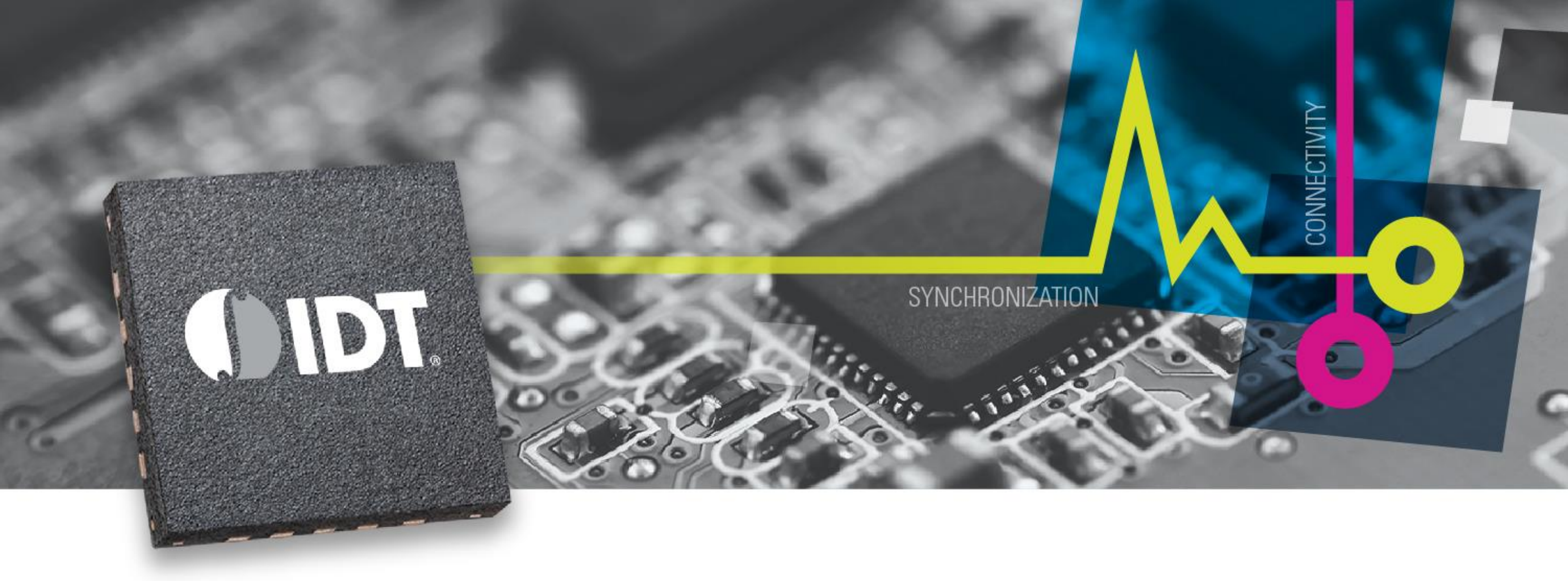


XO Categories rel. Temp. Control

- OCXO, Oven Controlled XO:
  - A control loop maintains the oven containing the XO at (nearly) constant temperature.
  - 5E-9 to 5E-8 over [-30°C to 60°C]
- DOCXO, Double Oven Controlled XO:
  - Two temperature controlled ovens, one inside the other.
  - 5E-11 to 5E-9 over [-30°C to 60°C]

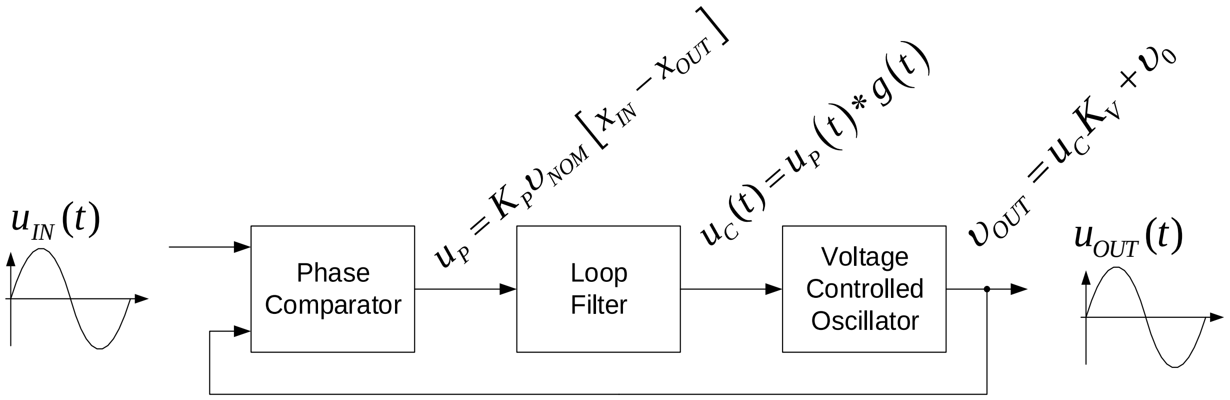






2. Phase-Locked Loops (PLL)

PLL: Working principle



$$u_{IN}(t) = A \cdot \sin\left\{2\pi\upsilon_{NOM}\left[t + x_{IN}(t)\right]\right\} = A \cdot \sin\left\{2\pi\upsilon_{IN}(t) + \varphi_{0,IN}\right\}$$

$$u_{OUT}(t) = A \cdot \sin\left\{2\pi\upsilon_{NOM}\left[t + x_{OUT}(t)\right]\right\} = A \cdot \sin\left\{2\pi\upsilon_{OUT}(t) + \varphi_{0,OUT}\right\}$$

- A phase lock loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal
  - Bringing the output signal back to the input signal for comparison is called a feedback loop
- By keeping the input and output phase in lock, this implies that the input and output frequencies are the same as well
- PLLs generally generate an output frequency that is a multiple, or even a fractional multiple, of the input frequency
  - May requires an integer, or fractional, divider on the feedback
  - May require an integer, or fractional, divider on the input as well

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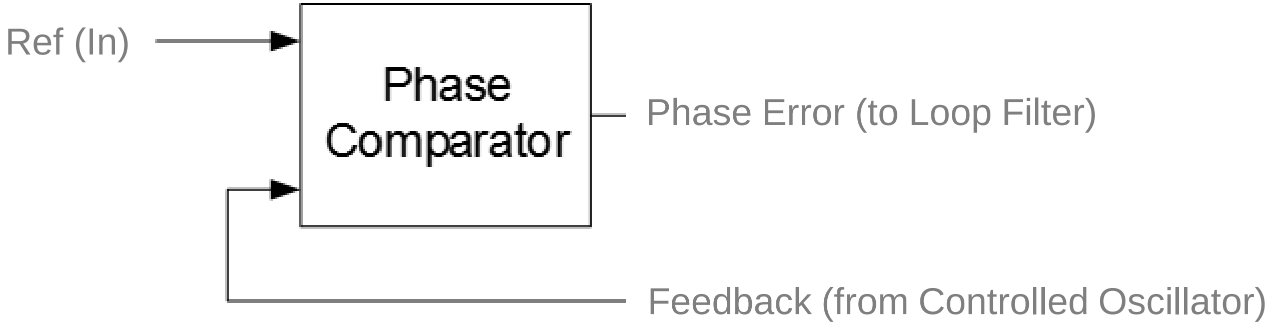
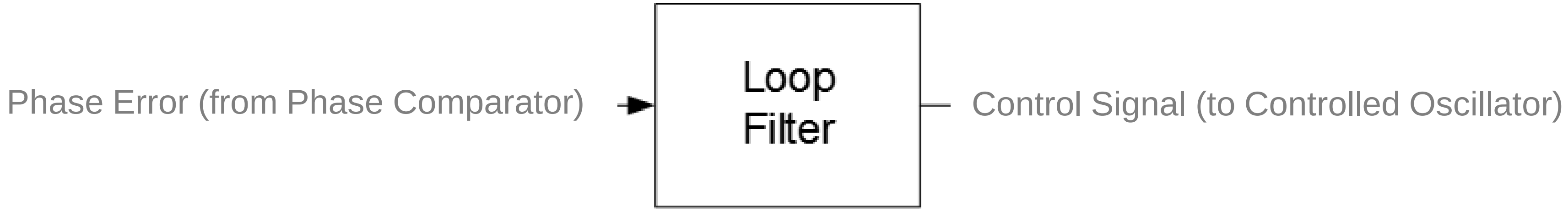
PLL: Phase Comparator



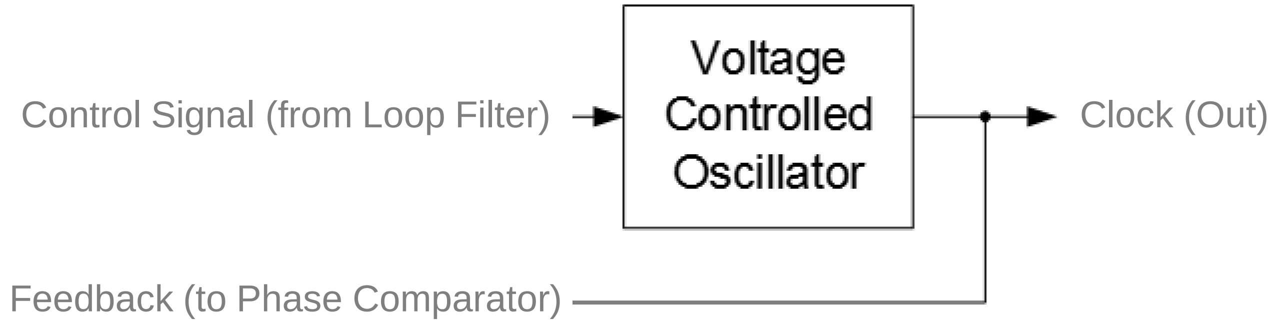
- The Phase Comparator establishes the “error” between the reference input and the clock output; using a feedback
- Most Digital PLLs (DPLLs) use a Time to Digital Converter (TDC) and Phase Frequency Detector (PFD) to measure the phase of the two clocks and produce a digital word representing the error
  - TDC can be looked at as a timestamper
- The TDC timestamps the reference and feedback edges, and the PFD mathematically tracks the phase offset between the selected reference and feedback clocks
- The measured phase difference can go well beyond 1 period, or Unit Interval (UI), of the reference and feedback clocks; thus, the phase comparator must be able to measure over a large range of multiple input/feedback clock periods
  - Various telecom standards define a jitter & wander tolerance requirement - the widest is defined is 18µspp
  - For example, if the input clock has a nominal period of 8ns (125 MHz), then the jitter tolerance requirement equates to ± 1125 UI

PLL: Loop Filter



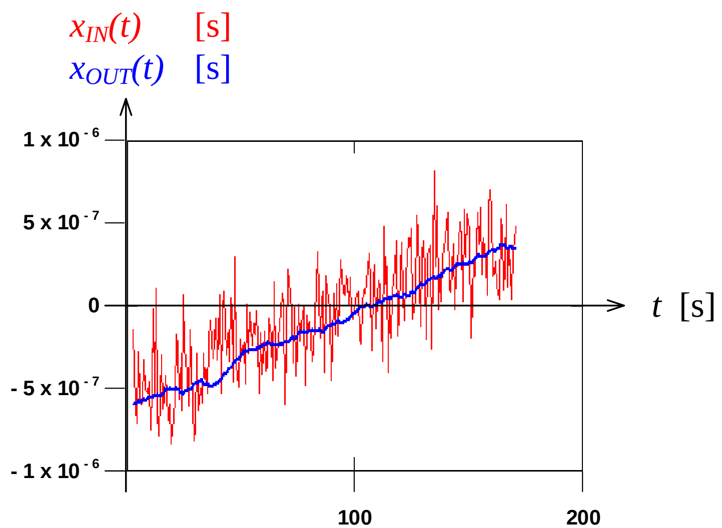
- The phase error is processed by the loop filter (LF)
  - LF is a combination of proportional and integral (PI) control, which generates a control signal for controlling the oscillator
- The LF determines the bandwidth (BW) of the PLL
  - Other functionality, such as phase slope limiting (PSL), locking range, and holdover functionality may be done as well
- Phase corrections mainly done through proportional path, along with any PSL
- Frequency offset, or drift corrections, is done through the integrator path, including damping (i.e. gain peaking control)

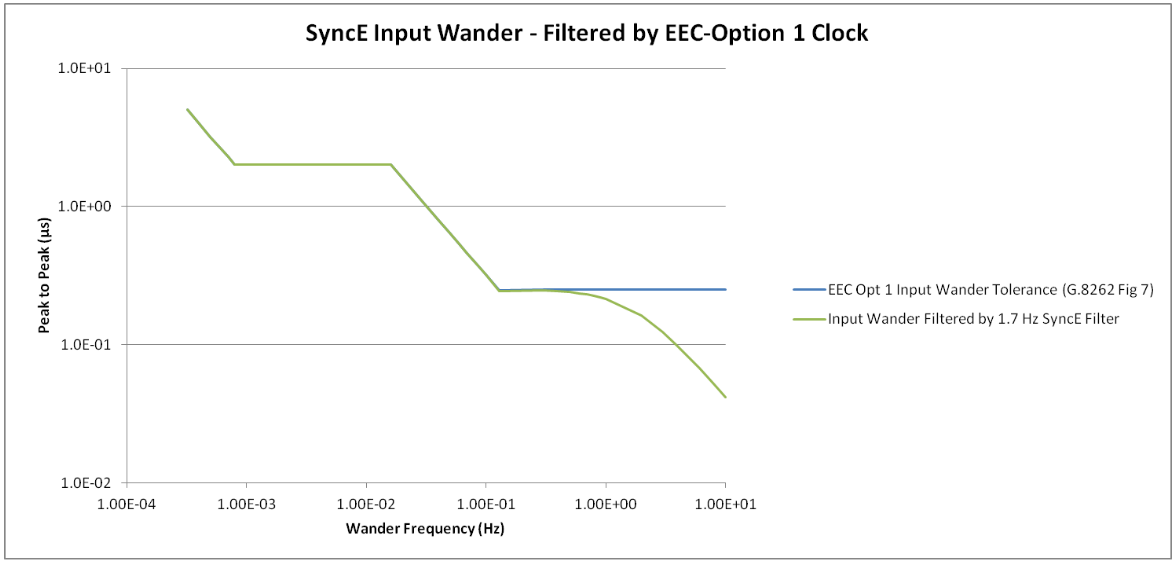
PLL: Controlled Oscillator



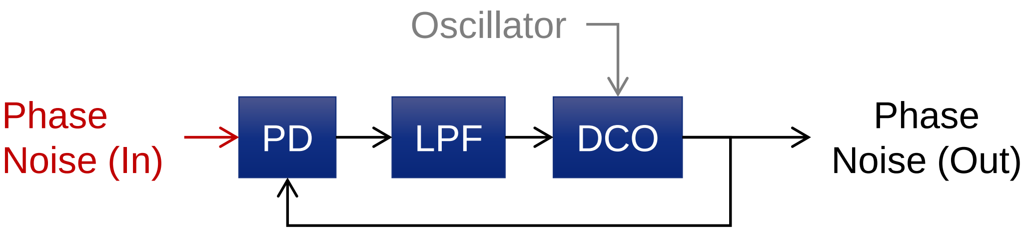
- The controlled oscillator uses the control signal to speed up or slow down the output clock
- Most DPLLs use a Digitally Control Oscillator (DCO) based on a free-running crystal oscillator (XO)
  - Control Signal is a digital word representing the fractional frequency offset (FFO)

PLL: Jitter & Wander filtering

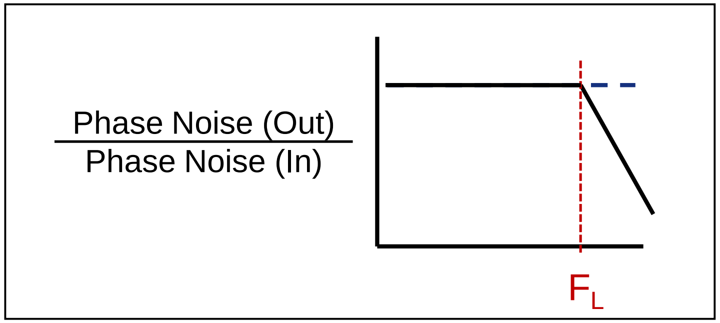


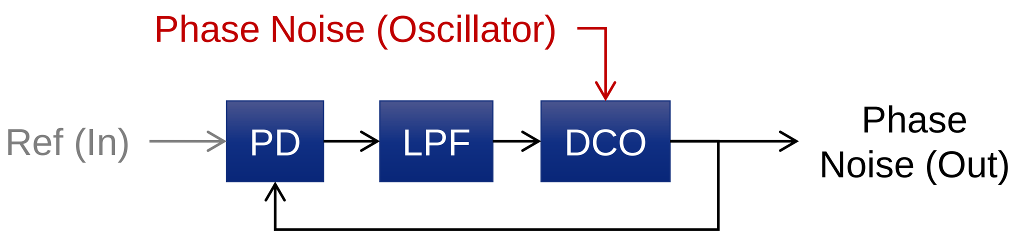


PLL: Response to Injected Noise

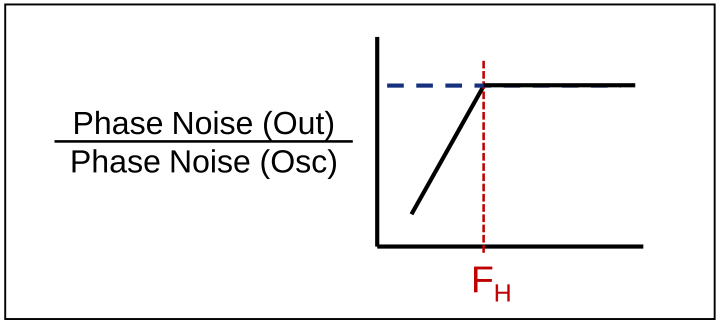


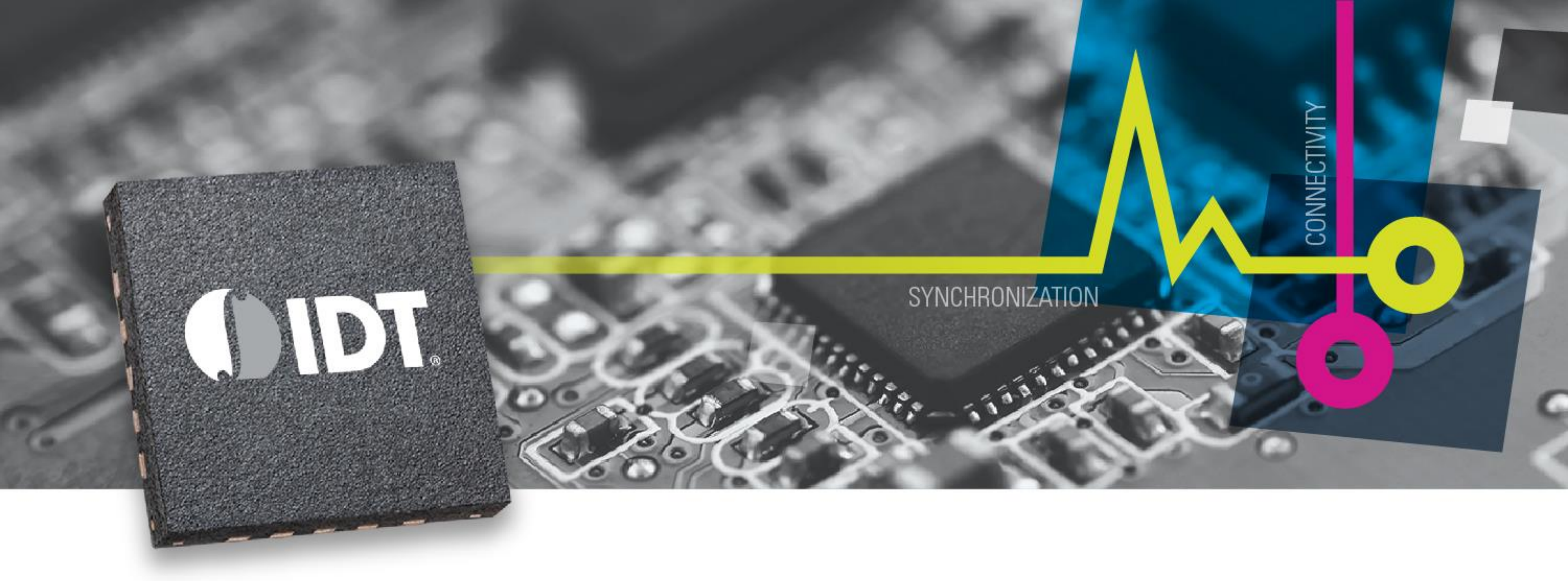
PLL is a low-pass filter for input noise





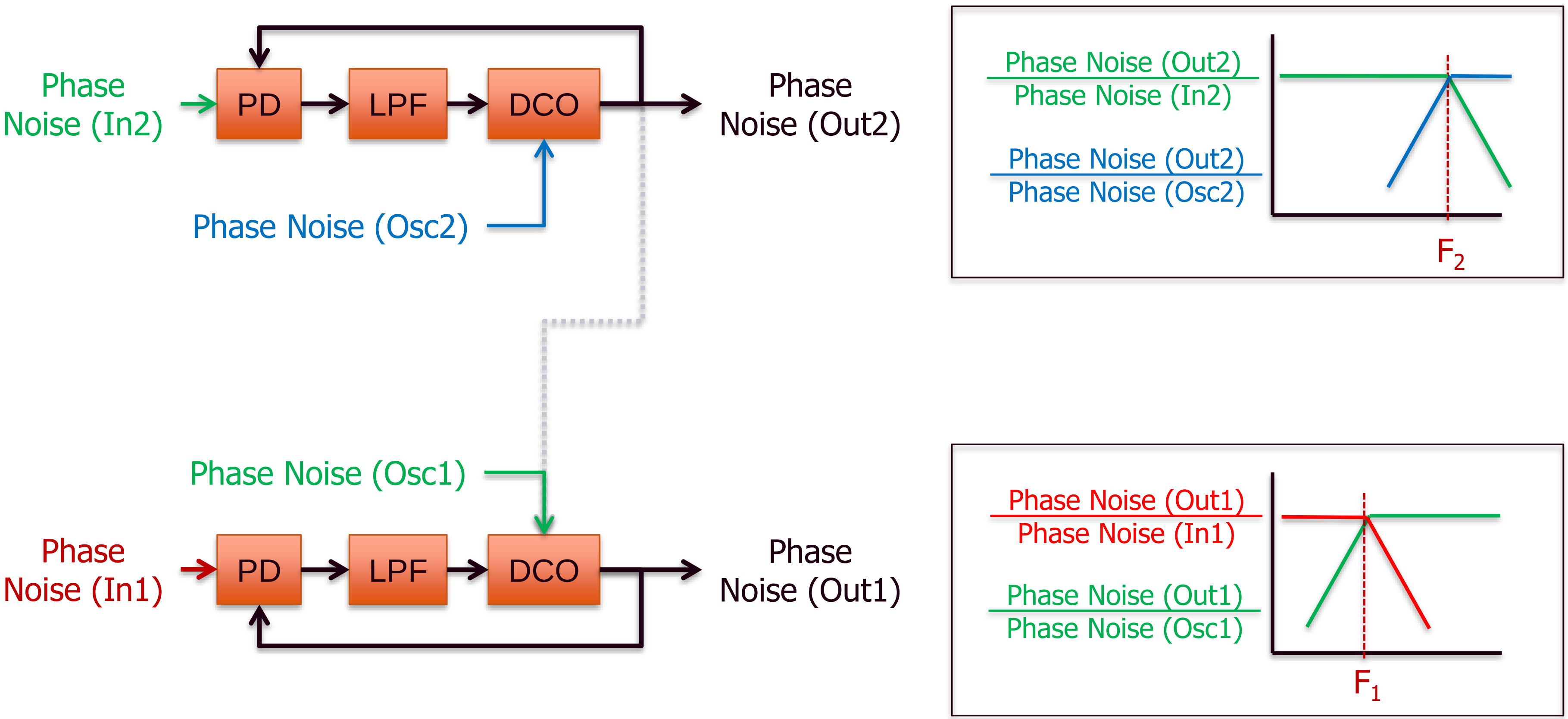
PLL is a high-pass filter for oscillator noise



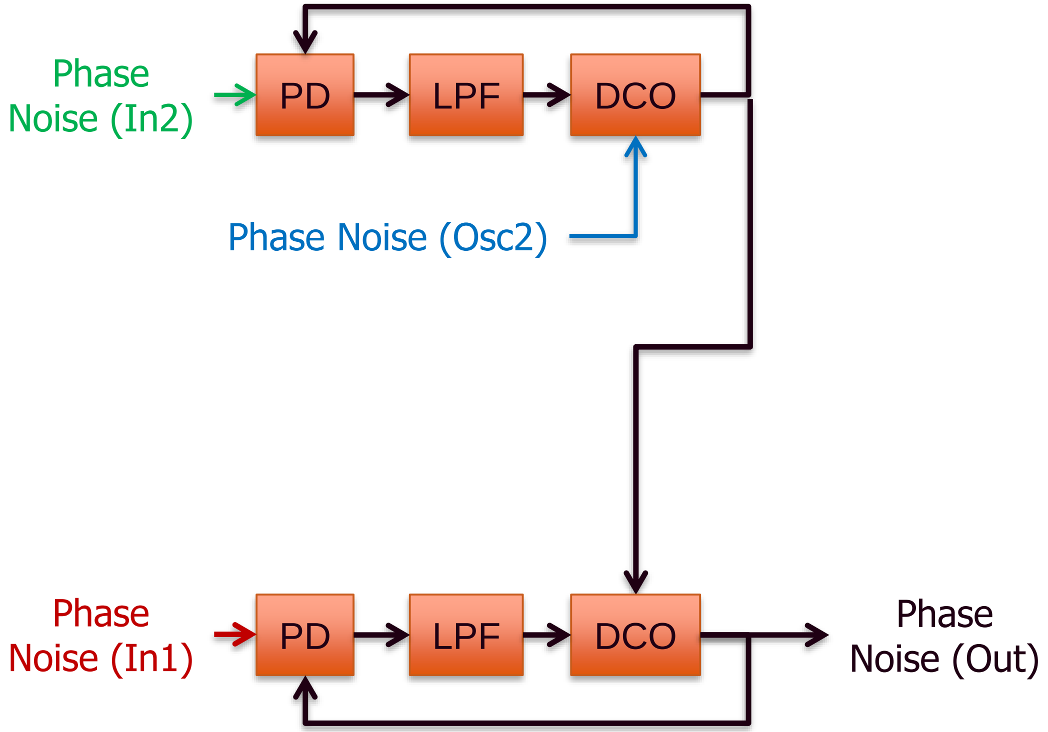


3. PLL with 2 Inputs

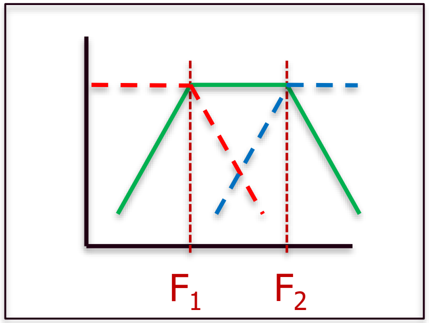
Combining two PLLs



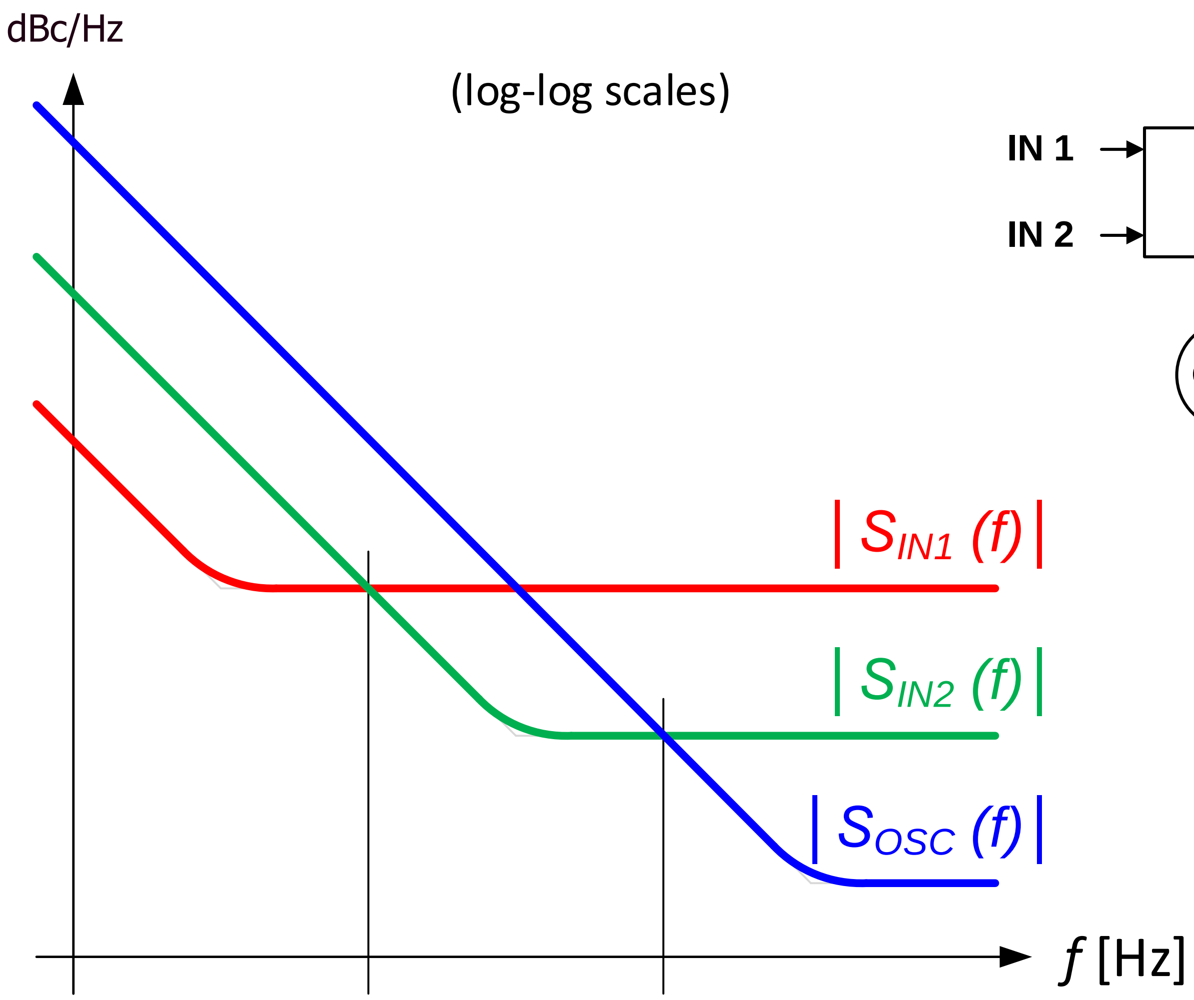
Two PLLs: Response to Injected Noise



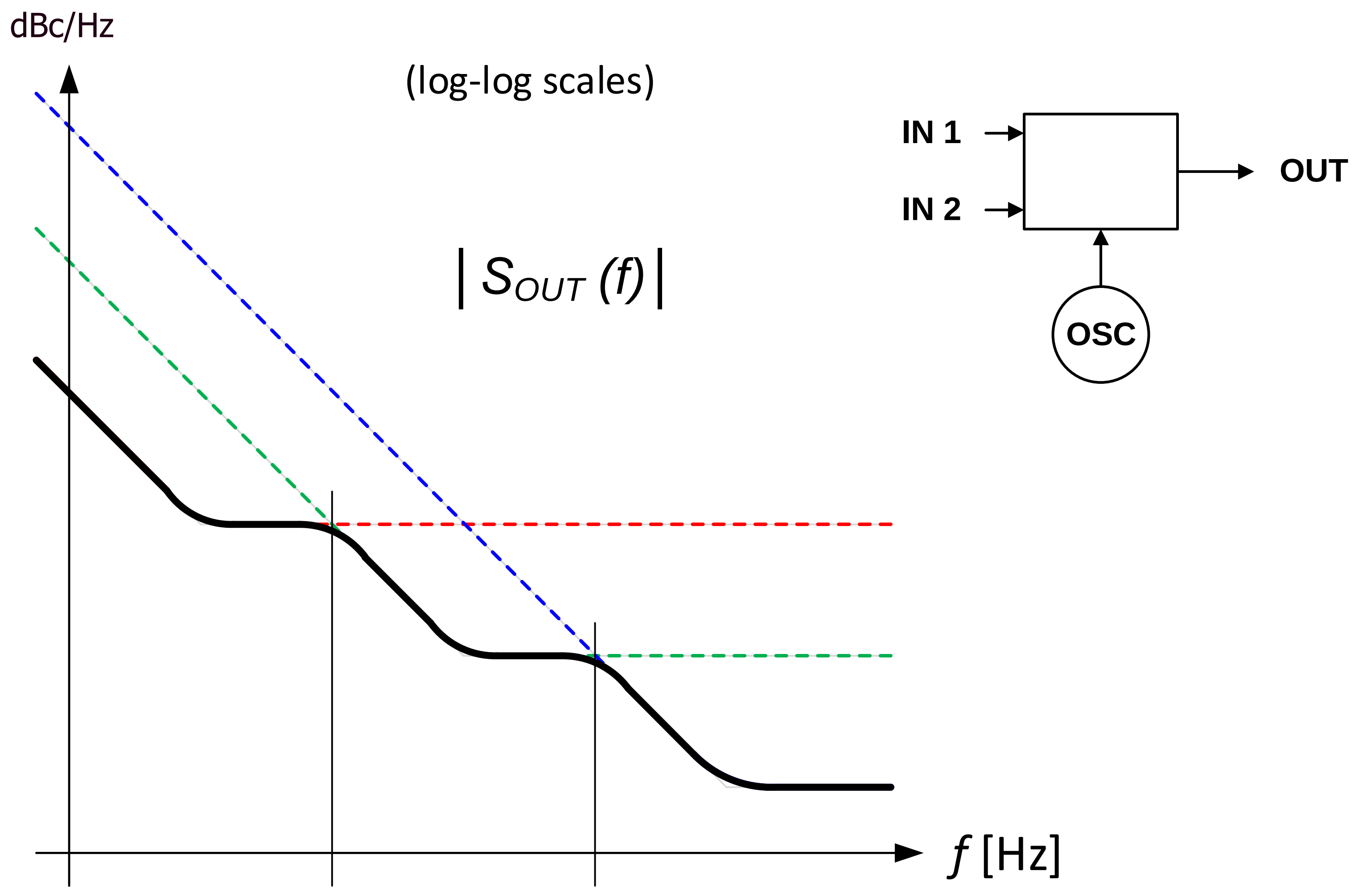
Band-pass filter for In2 Noise to Out



Two PLLs: Spectral densities (phase-time)



Two PLLs: Combined spectral densities



Physical Layer Support for Telecom Boundary Clock

- G.8273.2 calls for Telecom Boundary Clock (T-BC) to use the physical layer as the basis for the frequency of the PTP time clock
- G.8273.2 uses PRC/PRTC traceable physical layer frequency support for long term (24hrs) time holdover

G.8273.2

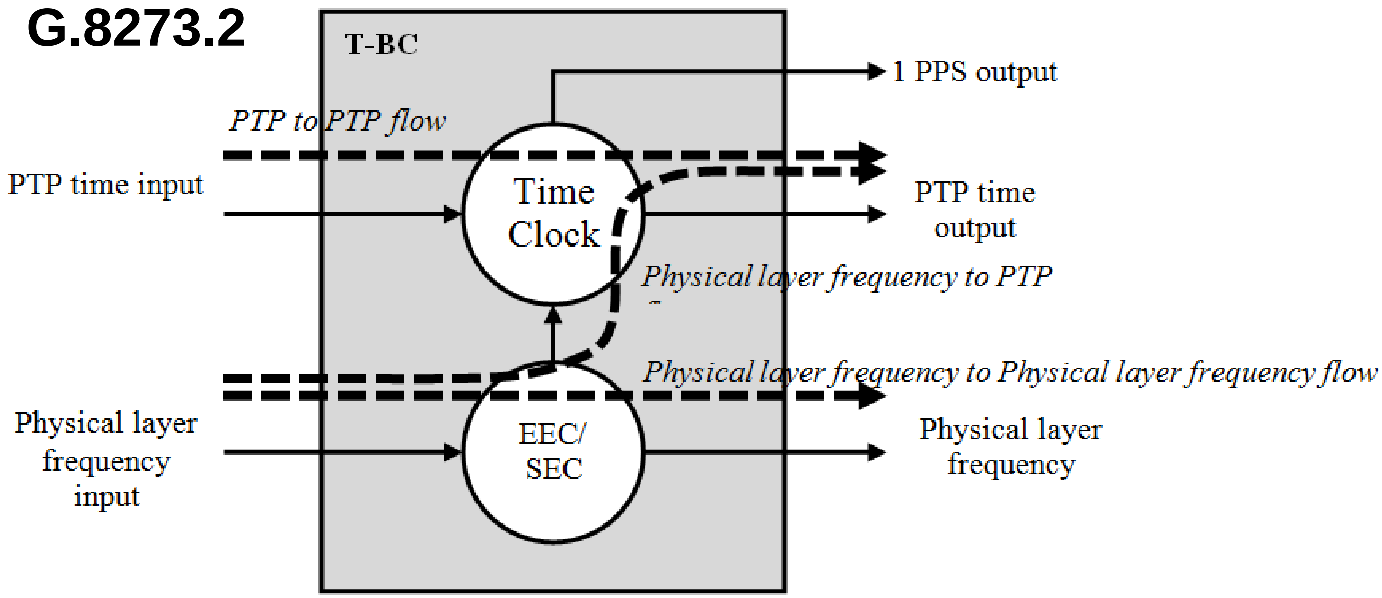
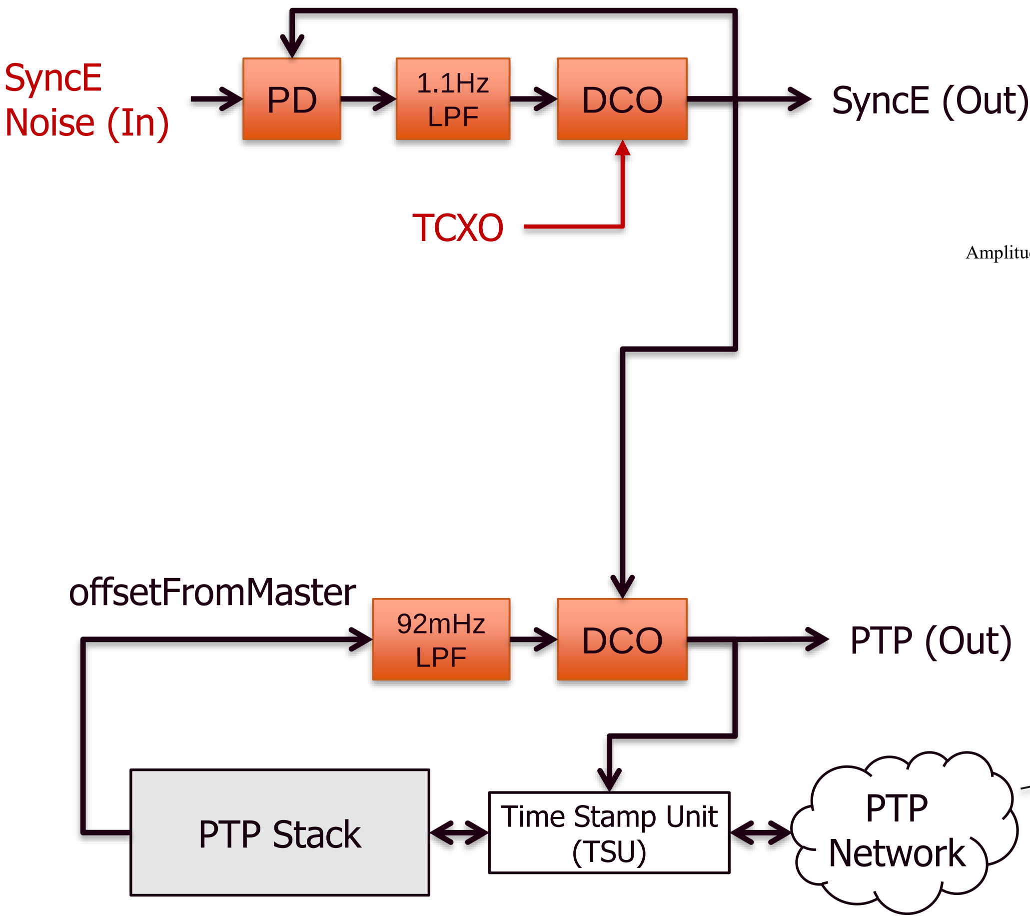
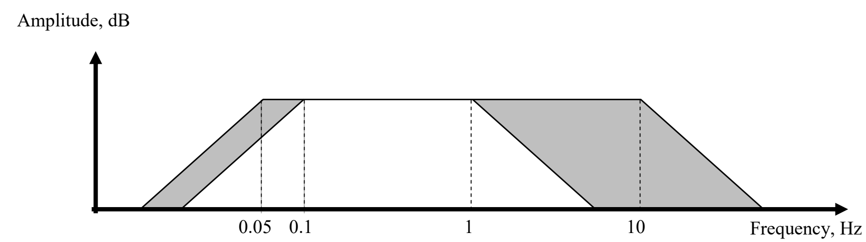


Figure III.5: Signal Flows through a T-BC

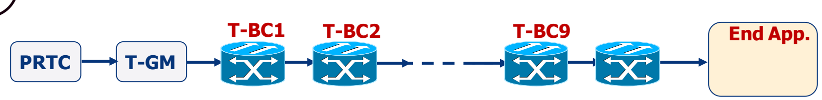
SyncE + IEEE 1588: Response to Injected SyncE Noise

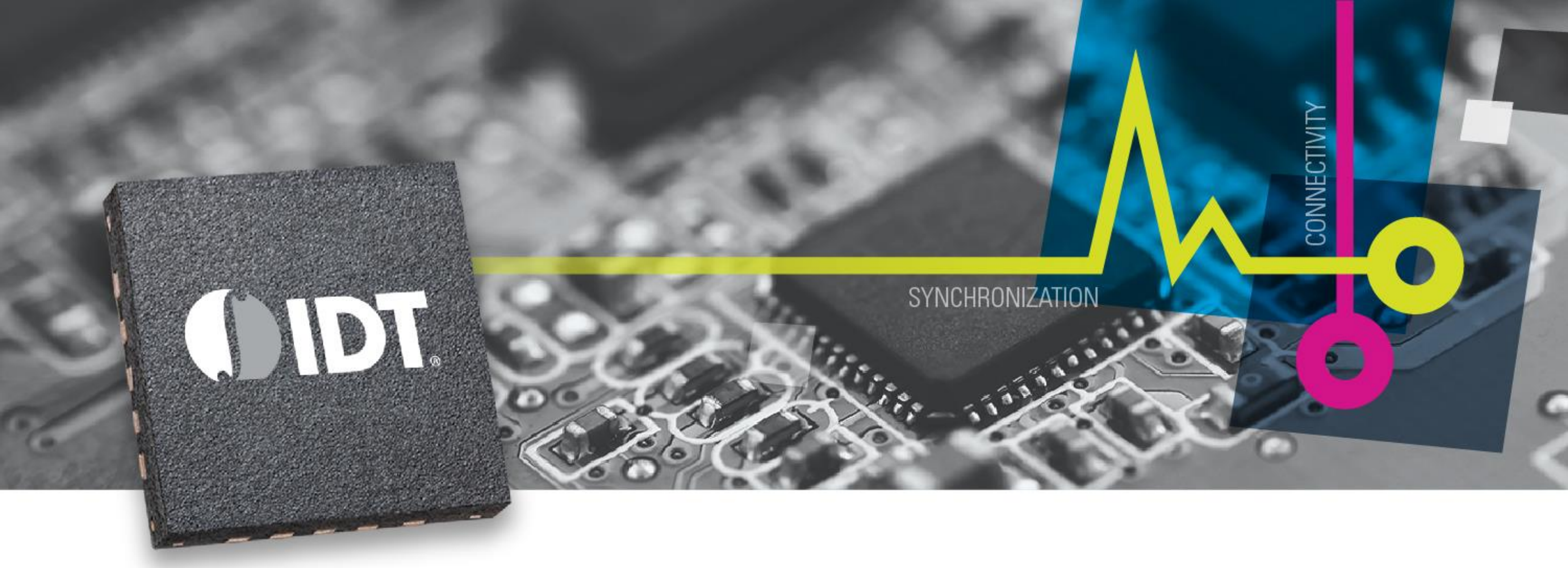


A band-pass filter for SyncE Noise to PTP (Out)



Very little PDV





Thank You

Analog Mixed Signal Product Leadership in Growth Markets