

WSTS-2017 Tutorial Session

Workshop on Synchronization in Telecommunications Systems San Jose, California, April, 2017

Presenters:

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Lee Cosart (Microsemi)

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Tutorial Outline



- Fundamentals of Synchronization and Introduction to Clocks
- Timing Reference Sources & Atomic Clocks
- Phase-Locked Loops and Oscillators
- Measuring and Characterizing Network Time
- Timing in Packet Networks
- Standards
- Concluding Remarks



FUNDAMENTALS OF SYNCHRONIZATION AND INTRODUCTION TO CLOCKS

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Fundamentals of Synchronization

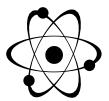


- Time and Frequency
 - Clocks and Oscillators
 - Alignment (frequency, phase, time)
- Fundamental need for Synchronization
 - Coordinated Signal Processing requires phase alignment
 - Writing a stream into and reading the stream from a buffer must be frequency aligned
 - Time-stamping events in geographically separated locations
- Examples

Time and Frequency

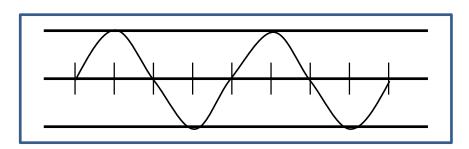


A clock is a frequency device based on physics



Provides "ticks" at precise intervals; Frequency is reciprocal of period

Electronic systems count "ticks" for time interval



"Time-Clock" provides the time elapsed since the "start"

Time is a combination of a signal (event) and a label (time value)

Time and Frequency



- Time Interval (e.g. 1 second) is based on a physical property of the Cesium atom
- Time is an artificial construct.
 - Choose an origin ("epoch") that people can agree on
 - Elapsed time interval from the origin.
 - Format (year/month/day/hour/min/sec...) [Time Zone]

Timescale	Epoch	Relationship	Leap Seconds	Other
TAI	Jan 1, 1958	Based on SI second	No	Continuous
UTC	Jan 1, 1972	TAI-UTC = 33sec	Yes	Discontinuous
UT-1	Jan 1, 1958	Earth's rotation	No	Astronomical
GPS	Jan 6, 1980	TAI – GPS = 19sec	No	Continuous
Loran -C	Jan 1, 1958	UTC + 23 sec	No	Discontinuous
Local	Jan 1, 1972	TAI-UTC = 33sec	Yes	Discontinuous, Based on Time zone offset
PTP	Jan 1, 1970	TAI – PTP = 10sec	No	Continuous
NTP	Jan 1, 1900	UTC	Yes	Discontinuous

"discontinuous" timescale allows for jumps related to leap seconds

Clocks and Oscillators

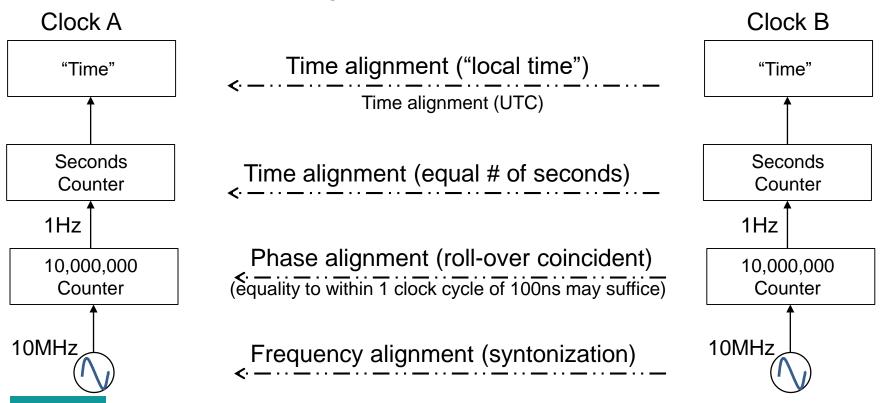


- Distinction is more in terms of emphasis
 - Both entities relate to time/frequency
 - Both entities have the notion of periodicity (time-base)
 - Both entities provide "edges", but
 - Clocks usually associated with edges (square waves) (digital)
 - Oscillators usually associated with waveforms (sine waves) (analog)
- Clock: Device/system that provides timing signals to other devices/systems
 - Emphasis is on time (time interval) accuracy
 - There is the notion of calibration (traceability to UTC)
 - A clock is a "disciplined" oscillator plus counting capability
- Oscillator: Component providing periodic signals
 - Emphasis is on frequency stability (temperature, aging)
 - Waveform integrity is important ("phase noise")
 - Oscillators are components of clocks

Time and Frequency

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- Aligning two time clocks (synchronization) implies:
 - Make frequency B = frequency A (syntonization)
 - Make phase B = phase A (e.g. roll-over instant of 10^7 counter)
 - Make seconds B = seconds A (elapsed time equal; same time origin)
 - Choose same formatting convention (and time-zone, etc.)



Fundamentals of Synchronization

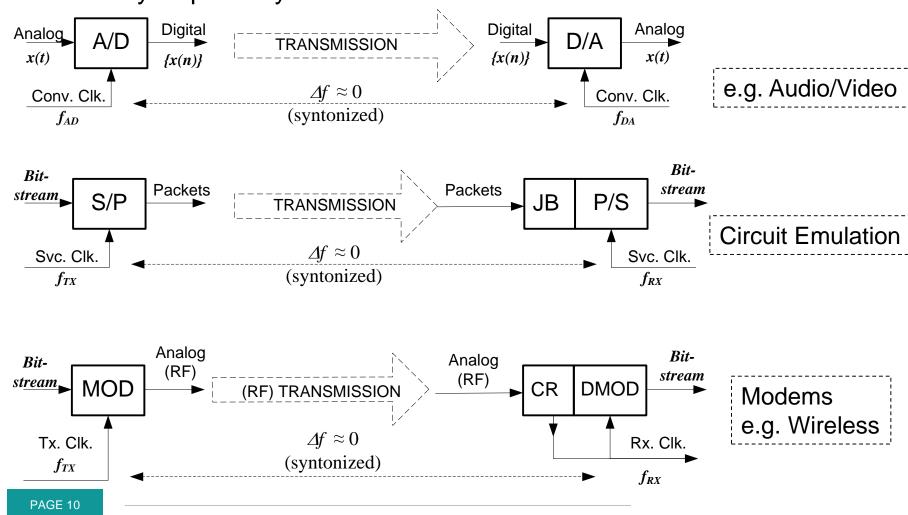


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Fundamental Need for Synchronization



Information has a temporal aspect (signals) — Digital Signal Processing inherently requires synchronization



Examples of single source, single destination

Fundamental Need for Synchronization QULSAR

- Multiple source single destination an example
- Device receives a combination of signal + interference $x(t) = a(t) + b(t + \delta)$
- Device has a "copy" of the interference b(t) but....error in synchronization results in an effective time-shift of copy
- Device subtracts the "copy" from its receive signal
- What could go wrong?

$$y(t) = x(t) - b(t) = x(t) + e(t)$$
 (signal + remnant)

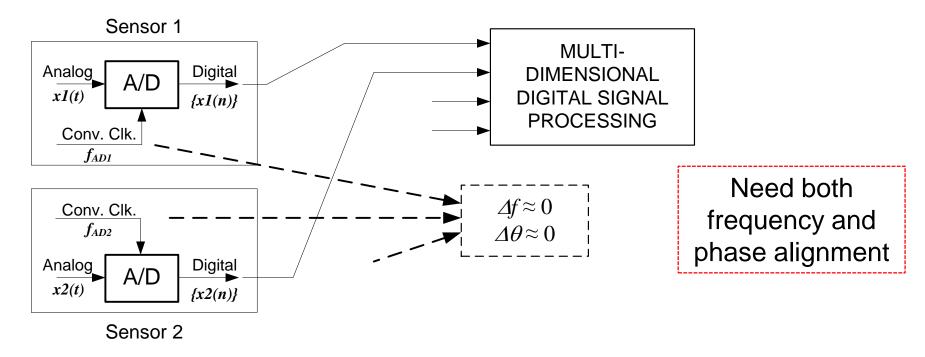
$$\sigma_e^2 = \sigma_b^2 \cdot (1 - r_b(\delta))$$

(power of remnant depends on autocorrelation of b(t) AND δ)

Bad synchronization leads to less than perfect cancellation of interference

Fundamental Need for Synchronization

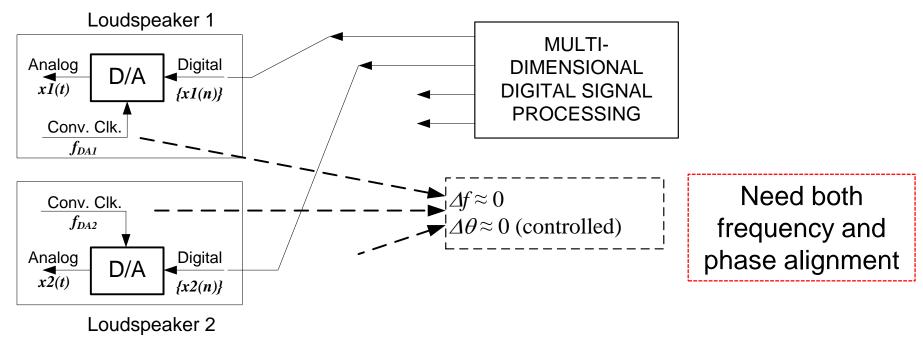




- Multiple sources, single destination (many, many, examples)
- Wireless: MIMO, eICIC, CoMP, etc., etc.
- Multimedia: audio/video, surround-sound, 3D video, etc., etc.
- Power: synchrophasors
- Geophysical applications (e.g. mapping strata for oil exploration)

Fundamental Need for Synchronization

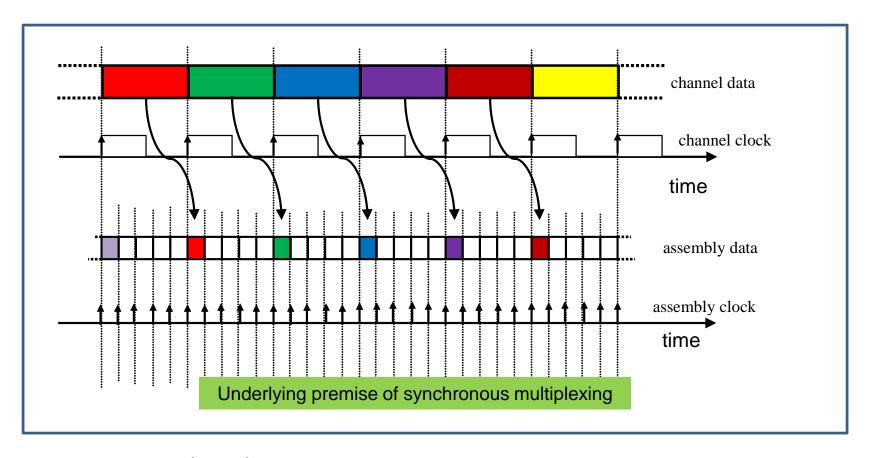




- Single source, multiple destinations (many, many, examples)
- Wireless: CRAN: BBU-RRH; Antenna arrays
- Multimedia: audio/video, surround-sound, 3D video, etc., etc.
- Power: relay control

Buffer Write-Read – Synchronous Multiplexing





- Predetermined (rigid) ratio between channel clock and assembly clock
- 1-to-1 correspondence between channel bits and allowed bit positions
- Fractional frequency difference between channel and assembly clocks = 0

Coordination of actions



- What if 2 persons in geographically separated locations are "simultaneously" accessing a common database (or document) that is on a server in a third geographical location?
- ◄ How can "order" be established by timestamping the actions using a common clock.
- Requires end-point synchronization to this common clock.
- Many examples (distributed data base, shared documents, stock trades, sensor fusion, etc., etc.)

Fundamentals of Synchronization



- Time and Frequency
 - Clocks and Oscillators
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- Fundamental need for Synchronization
 - Coordinated Signal Processing requires phase alignment
 - Writing a stream into and reading the stream from a buffer must be frequency aligned
 - Time-stamping events in geographically separated locations
- Examples (in Telecommunications)

Fundamental need for Synchronization



- Timing Alignment is Fundamental in Telecommunications
 - Digital transmission requires symbol-timing alignment
 - Digital network require synchronization to emulate analog channels
 - Circuit Emulation (CBR over packet) requires timing alignment
 - Wireless (Cellular) requires timing alignment
 - Multimedia requires timing alignment
- Timing in Circuit-Switched (TDM) Networks
 - Synchronous time-division multiplexing

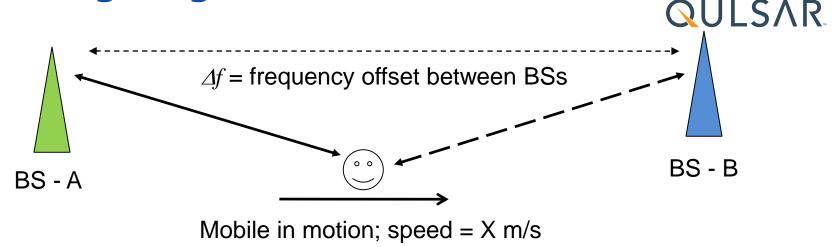
Timing alignment implicit in Circuit Emulation





- Network impairments: delay, <u>packet-delay-variation (PDV)</u>, discarded packets
- Jitter buffer size: large enough to accommodate greatest (expected) packet-delay-variation. Packet loss concealment is not an option.
- Causes of packet "loss":
 - Network drops packets (bit errors, congestion)
 - Jitter buffer empty/full (excessive packet-delay-variation)
- Key to <u>Circuit Emulation</u>:
 - Ensure packet loss is (essentially) zero.
 - Make RX and TX service clocks "equal".
 - Note: If RX ≠ TX then jitter buffer is going to overflow/underflow

Timing Alignment in Wireless



- Mobile in motion (X m/s) introduces a Doppler shift (X/c)
 - When hand-over occurs, the mobile must reacquire carrier frequency
 - Large ∆f compromises the reliability of hand-over
- Modern Wireless (LTE) requires stringent timing to support special services/functions
 - BS-A and BS-B can cooperate for providing enhanced bandwidth to mobile
 - Frequency as well as relative phase



INTRODUCTION TO CLOCKS

Introduction to Clocks



- Clocks and Oscillators
- Fundamental Clock Concepts and Metrics
 - Time Error (TE) and Time Interval Error (TIE)
 - MTIE
 - TDEV

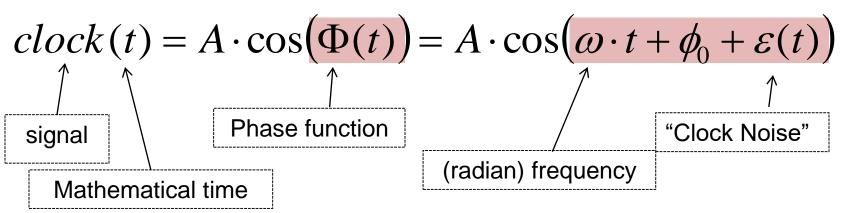
Clocks and Oscillators



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Common Mathematical Models





- A: Amplitude of signal. Does not figure in timing metrics.
- ϕ_0 : Initial phase. Depends on choice of time origin. Usually assumed to be 0.
- $\varepsilon(t)$: Can be further decomposed into different categories such as frequency error, frequency drift, and random noise components
- ideal periodic signal: $\Phi(t)$ is a linear function of $t(\varepsilon(t) \equiv 0)$

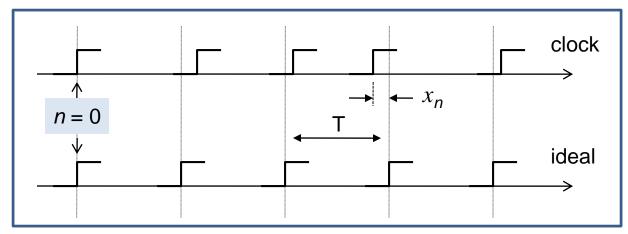
$$x(t) = a_0 + y \cdot t + \left(\frac{1}{2}\right) \cdot D \cdot t^2 + \phi(t)$$

$$x(nT_s) = a_0 + y \cdot nT_s + \left(\frac{1}{2}\right) \cdot D \cdot (nT_s)^2 + \phi(nT_s)$$
Time Erro
Models

Time Error

Clock Metrics – Basics: Time Error

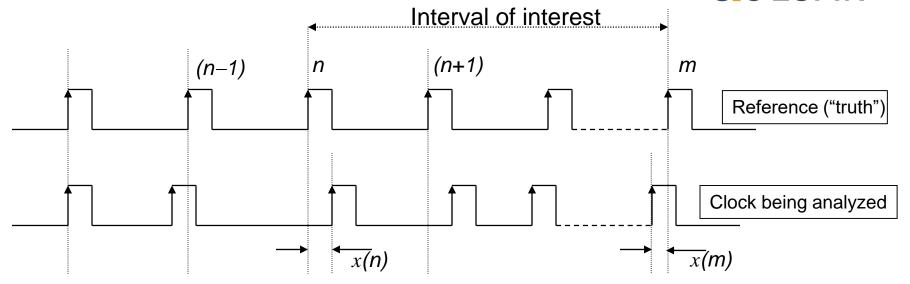




- Clock signals are (<u>almost</u>) periodic (<u>nominal</u> period ~ T)
- Time Error (Phase Error):
 - Edge does not line up phase error (expressed in time units)
- **▼** Time Error Sequence : $\{x_n\}$ or $\{x(n)\}$
 - All clock metrics derived from time error sequence
 - Note: the time error varies "slowly" so we can divide down to a convenient rate (However: careful when dividing down – aliasing)
 - Common assumption: $x_0 = 0$.

Time Interval Error





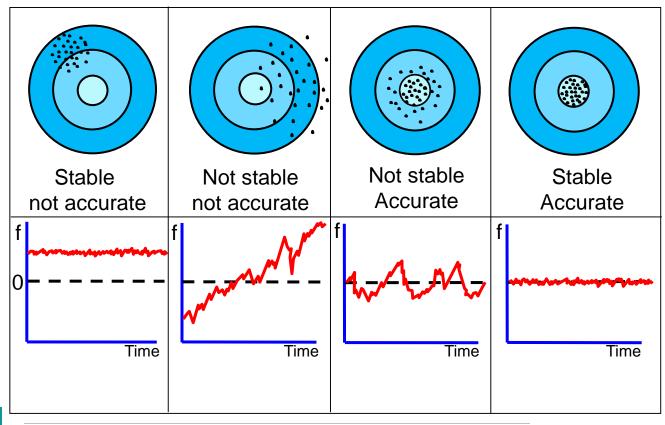
- Consider an interval of interest (e.g. 100m dash)
- Duration measured by ideal clock ("truth") : $(m n) \cdot T_S$
- *Error* in measurement of same interval by clock being analyzed:

$$TIE(m, n) = x(m) - x(n)$$

Accuracy and Stability



- Accuracy: Maximum (freq., phase or time) error over the entire life of the clock
- Stability: (Freq., phase or time) change over a given observation time interval
- Stability is expressed with some statistical dispersion metric as a function of observation interval (e.g. ADEV, TDEV, MTIE, etc.)



Clock Metrics – MTIE and TDEV





A measure of peak-to-peak excursion expected within a given interval, τ MTIE (τ is a parameter). The observation interval is scanned with a moving window of duration τ and MTIE(τ) is the maximum excursion.

Given a set of N observations $\{x(k); k=0,1,2,...,(N-1)\}$, with underlying sampling interval τ_0 , let $\tau = n \cdot \tau_0$ ("window" = n samples; n = 1, 2, ..., N).

Peak-to-peak excursion over *n* samples starting with sample index *i* is:

$$peak - to - peak(i) = \{ \max_{k=i}^{k=i+n-1} x(k) - \min_{k=i}^{k=i+n-1} x(k) \}$$

 $\mathsf{MTIE}(n)$, or $\mathsf{MTIE}(\tau)$, is the largest value of this peak-to-peak excursion:

$$MTIE(n) = \max_{i=0}^{N-n} \left\{ \max_{k=i}^{k=i+n-1} x(k) - \min_{k=i}^{k=i+n-1} x(k) \right\}$$

Clock Metrics - MTIE and TDEV

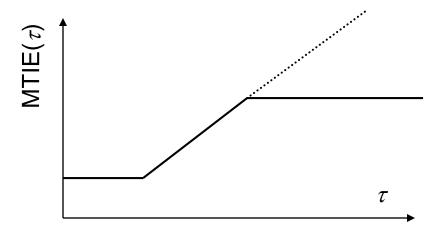




MTIE is a useful indicator of the size of buffers and for predicting buffer overflows and underflows.



Buffer size > MTIE(τ) implies that overflow/underflow unlikely in any interval < τ Buffer size = MTIE(τ) implies that overflow/underflow occurs approx. every τ seconds



Observations regarding MTIE:

- monotonically increasing with τ
- linear increase indicates freq. offset
- for small τ , MTIE(τ) \leftrightarrow jitter
- for medium τ , MTIE(τ) \leftrightarrow wander
- for large τ, indicates whether "locked"

Clock Metrics – MTIE and TDEV



A measure of stability expected over a given observation interval, τ (τ is a parameter).

Given a set of N observations $\{x(k); k=0,1,2,...,(N-1)\}$ with underlying sampling interval τ_0 , let $\tau = n \cdot \tau_0$ ("window" = n samples; n = 1, 2, ..., N).

$$\sigma_{x}(\tau) = TDEV(\tau) = \sqrt{\frac{1}{6n^{2}(N - 3n + 1)} \sum_{j=0}^{N-3n} \left[\sum_{i=j}^{n+j-1} (x_{i+2n} - 2x_{i+n} + x_{i}) \right]^{2}}$$
Conventional Definition

for $n=1,2,..., \frac{N}{2}$

Note: $x(k) \Leftrightarrow x_k$

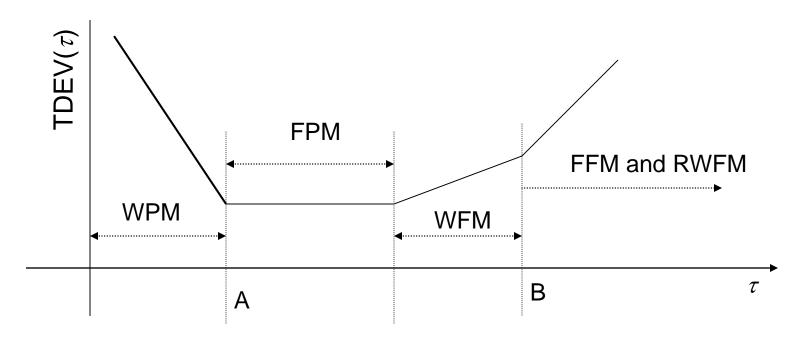
TVAR = square of TDEV TVAR = square of TDEV Modified Allan Variance (related to TDEV) : $\sigma_y(\tau) = \frac{\sqrt{3}}{\tau} \sigma_x(\tau)$

TDEV suppresses initial phase and frequency offset and quantifies the strength of the frequency drift and noise components {i.e. $\varepsilon(t)$ }

TDEV provides guidance on the noise process type

Implication of TDEV(τ) versus τ





"Phase coherence" for up to A sec.

 \Rightarrow Keep PLL time constants less than A sec.

Phase Flicker Floor

"Frequency coherence" for up to B sec.

⇒ Keep FLL time constants less than B sec.

Frequency Flicker Floor

Stratum Levels - Telecom



Stratum level represents the intrinsic accuracy of a clock

```
- Stratum-1: 1x10^{-11} (one part in 10^{11})
```

- Stratum-2: 1.6x10⁻⁸ (16 parts per billion, ppb)
- Stratum-3: 4.6x10⁻⁶ (4.6 parts per million, ppm)
- Stratum-4: 32x10⁻⁶ (32 parts per million, ppm)
- Implication:

output frequency is <u>always</u> accurate to xxx even if the reference fails and the clock goes into an autonomous mode of operation

Normal operation:

output frequency is as accurate as the reference frequency (locked condition) – maintain a hierarchy in any chain of clocks (why?)

Time-constant achievable:

```
ST2 of the order of 10<sup>5</sup> sec (bandwidth ~mHz)
ST3E of the order of 10<sup>3</sup> sec (bandwidth ~mHz)
ST3 of the order of 10 sec (bandwidth ~Hz)
ST4 of the order of 1 sec (bandwidth ~10Hz)
```

Order of magnitude!

Concluding Remarks



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 - MTIE and TDEV
- Examples

Thank you ...

Questions?

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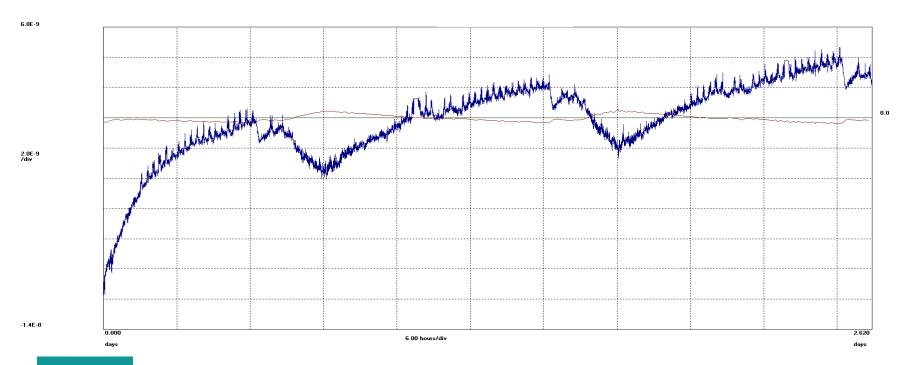
Backup Slides

Time and Frequency



- Does an oscillator labelled "10MHz" provide a 10MHz output?
 - Two good oscillators measured over >2 days
 - Frequency is close to 10MHz BUT not exactly equal nor constant

Symmetricon 1 intermental Analyzer
Fractional frequency offset; Fs=99.65 mHz; Fo=20.00 MHz; 2013/11/22; 17:06:17
1 [blue]: Agilent 53220A; Test 49; M6164LF; 20 Mhz; Samples: 22954; Gate: 10 s; Glitch: 10.00 mHz; Start: 400; Freq/Time Data Only; Rakon Sample M6164LF Mercury; 2013/11/22; 17:06:17
2 [red]: Agilent 53220A; Test 50; STP 3032 LF; 10 MHz; Samples: 22954; Gate: 10 s; Glitch: 10.00 mHz; Start: 400; Freq/Time Data Only; Rakon OCXO STP 3032 LF; 2013/11/22; 17:06:17

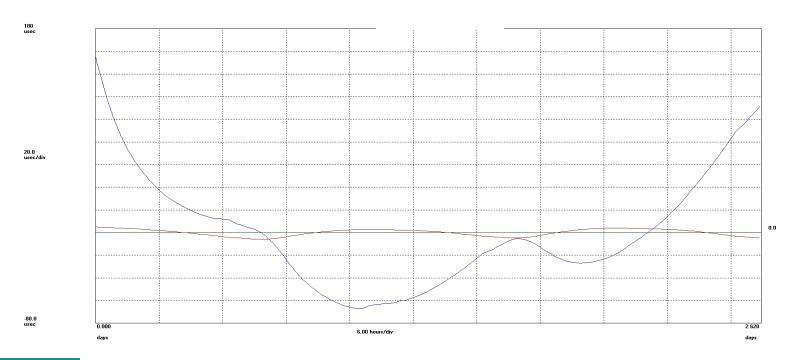


Time and Frequency

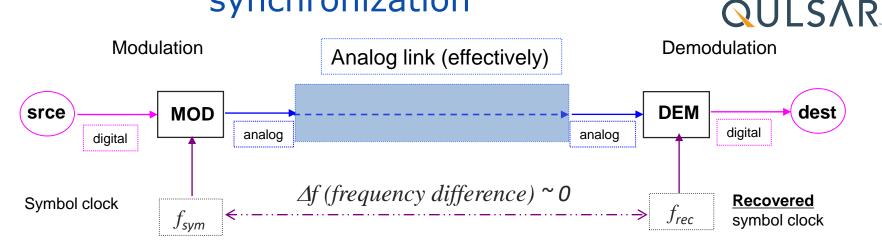


- Does an oscillator labelled "10MHz" provide a 10MHz output?
 - Two good oscillators measured over >2 days
 - Phase error accumulation is small BUT not exactly zero nor constant

Symentricon TimeMonitor Analyzer
Phase devisition in units of time: Fs-99.65 mHz; Fo-20.000001 MHz; 2013/11/22; 17:06:17
1 (blue): Agilent 53220X; Test: 49; M6164LF; 20 Mhz; Samplex: 22994; Gate: 10 s; Giltich: 10.00 mHz; Start: 400; Freq/Time Data Only; Rakon Sample M6164LF Mercuy; 2013/11/22; 17:06:17
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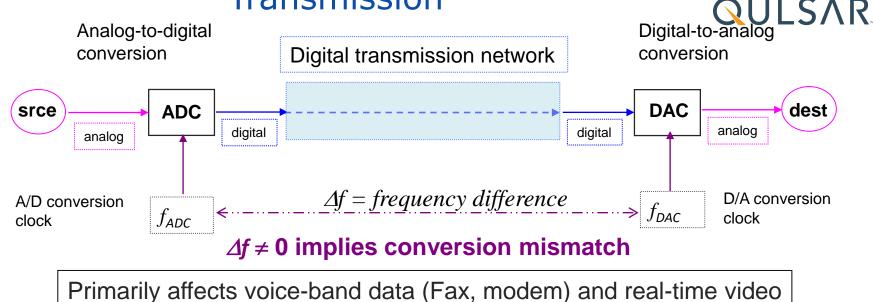


Data transmission schemes require synchronization



- Source/Destination : modulator and demodulator
- Transmitter (modulator) uses a particular symbol clock
 - receiver (demodulator) must extract this clock ($\Delta f \sim 0$) for proper data recovery
- The "Analog link" must, effectively, mimic an analog wire pair
 - Frequency translation (e.g. DSB-AM) is benign, Doppler (pitch modification effect, PME) is not benign (△f ~ Doppler)

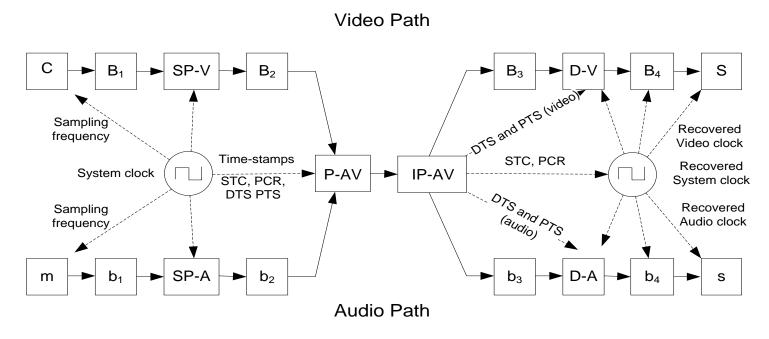
Timing Alignment required in Voice-Band Transmission



- Source/Destination : Voice/video/fax terminal
- The digital transmission network emulates an analog circuit (the original circuit emulation)
- Impact of frequency difference (△f):
 - Eventually buffers will overflow/underflow (e.g. slips) ("obvious")
 - Pitch Modification Effect (PME) (analogous to Doppler) makes recovered symbol clock ≠ transmit symbol clock (not so "obvious")
 - Recovered waveform ≠ original waveform (more than just additive noise)

Timing Alignment in Multimedia





- Frequency offset (wander) between audio and video sampling results in loss of lip-sync
- Frequency offset (wander) between send-side and receive-side system clock results in freeze (video), breaks (audio), and possible loss of lip-sync

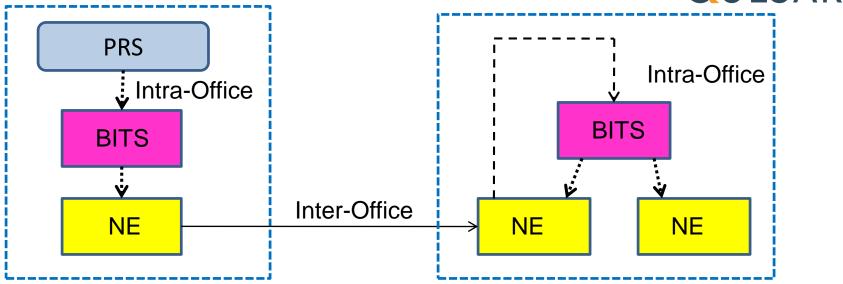
Timing in TDM Networks



- Synchronization is essential for synchronous multiplexing
 - To avoid information loss
- Synchronous multiplexing assemblies are used as carriers of timing information (DS1/E1, SONET/SDH)
 - The recovered clock is used as a reference for the BITS
 - The transmit signals must meet the "sync" mask for timing information
- Some Thumb Rules in TDM Networks:
 - Asynchronous multiplexing can preserve timing (up to a point) if done correctly
 - Bearer signals (DS1/E1) in asynchronously multiplexed assemblies (e.g. DS1 in DS3) can be used as carriers of timing
 - DS1/E1 bearer signals in SONET/SDH are <u>not</u> suitable as carriers of (good) timing because SONET/SDH encapsulation of DS1/E1 was done in a way that protects data but not (good) timing information

Distribution of timing (frequency)

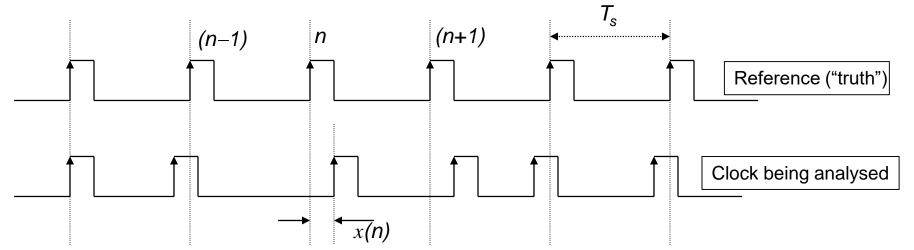
QULSAR



- PRS: Primary Reference Source provides stratum-1 quality output signal
- BITS: Building Integrated Timing Supply (also TSG Timing Sig. Gen.)
 - Provides clock reference to the different NEs in the CO
 - Accepts a reference input and performs clock-noise filtering (removes jitter/wander)
- NE: Network Element (e.g. SONET) uses BITS timing for its outputs
 - Recovers clock from incoming signal and provides a reference for the BITS

Time Error





Basic premises:

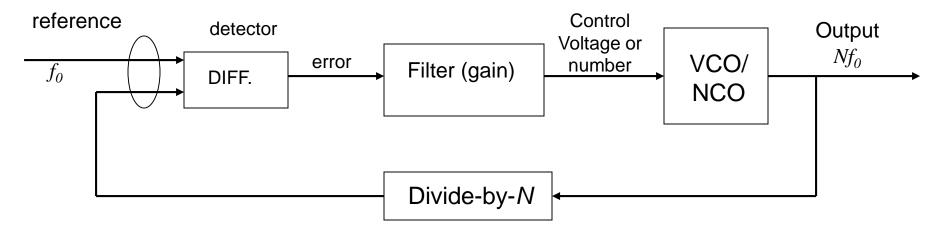
- Both reference and clock being analyzed have same nominal period, T_S
- The *nominal* value for x(n) is zero (or a constant)
- $T_0 = 0$ (common assumption) $\Rightarrow x(n) = n \cdot T_S T_n$

The discrete-time signal $\{x(n)\}$ is the "Time Error" (TE) and is the basis for quantifying the performance of the clock (relative to reference)

 $\{x(n)\}\$ can be viewed as the samples of a (analog) signal, x(t), taken every T_s seconds (implied sampling rate = $f_s = 1/T_s$) [Think DSP]

Loops and Holdover

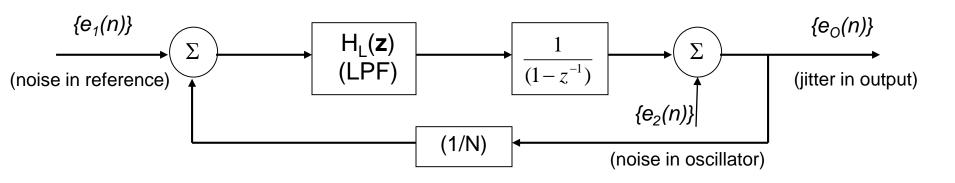


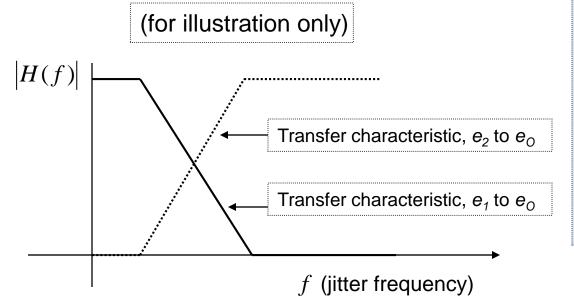


- Closed loop to discipline oscillator to align with reference
- What if reference fails ... Holdover operation
 - retain the last "good" value for control voltage/value
- What happens then?
 - frequency initially "good" (assuming instantaneous operation)
 - drift away (aging, temperature, noise, etc.)
 - "stable" value will be better than value associated with stratum
 - quality of oscillator becomes the determining factor

Analytical Model of Locked Loop







- High-freq. Noise (jitter) in output depends on the oscillator.
- Low-freq. noise (wander) depends on the reference.
- Narrow-band (LPF) implies a long time-constant.
- How large time-constant can be is governed by TDEV(τ) of oscillator and reference (flicker floor)