Phase Holdover Challenge – Next generation Modules

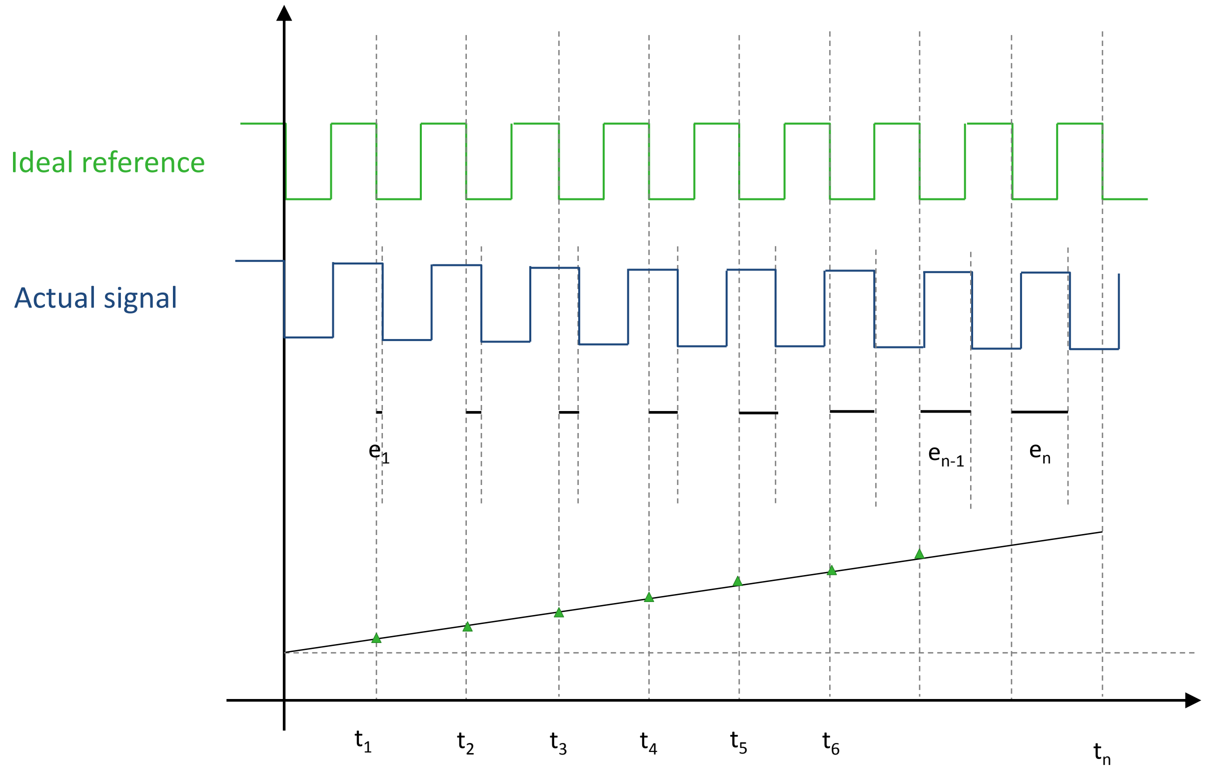
rakon

Presenter: Cyril Datin -R&D Manager-

Workshop on Synchronization and Timing System

WSTS 2016

Time alignment



frequency f_0

frequency f_1

Time Error is a sequence $\{e_n\}$

Time Interval Error is a cumulation of time error over period of observation

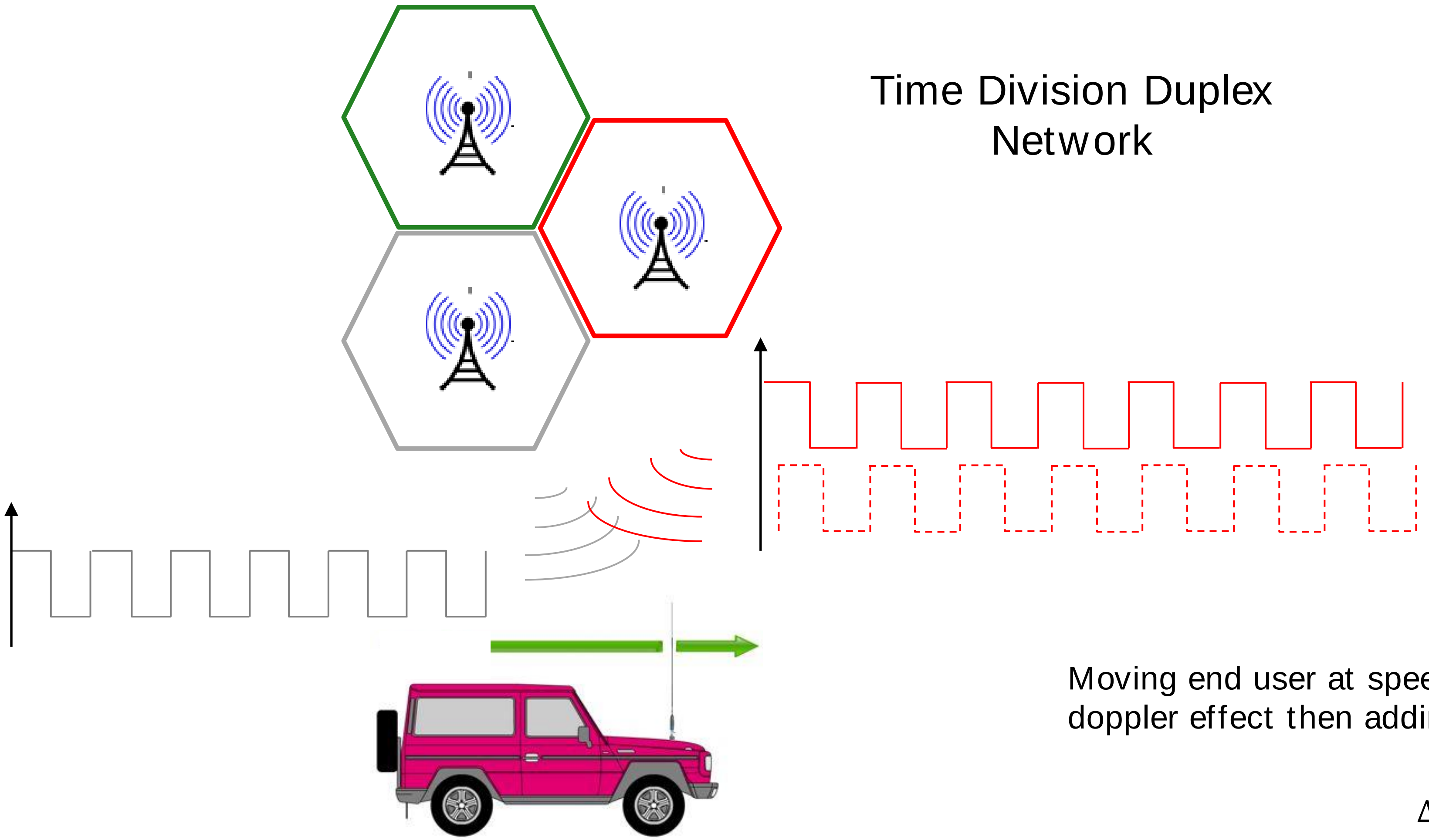
f_0 and f_1 being constant, the TIE -the cumulation of time error- **is linear over time**
This cumulation is called **time holdover x(t)**

- **Time Error:** measure the difference between 2 clocks
- **Time Interval Error:** measure the dynamic error **dTe**

Why does network require time alignment?

rakon

Time Division Duplex Network



Signal at frequency f_0

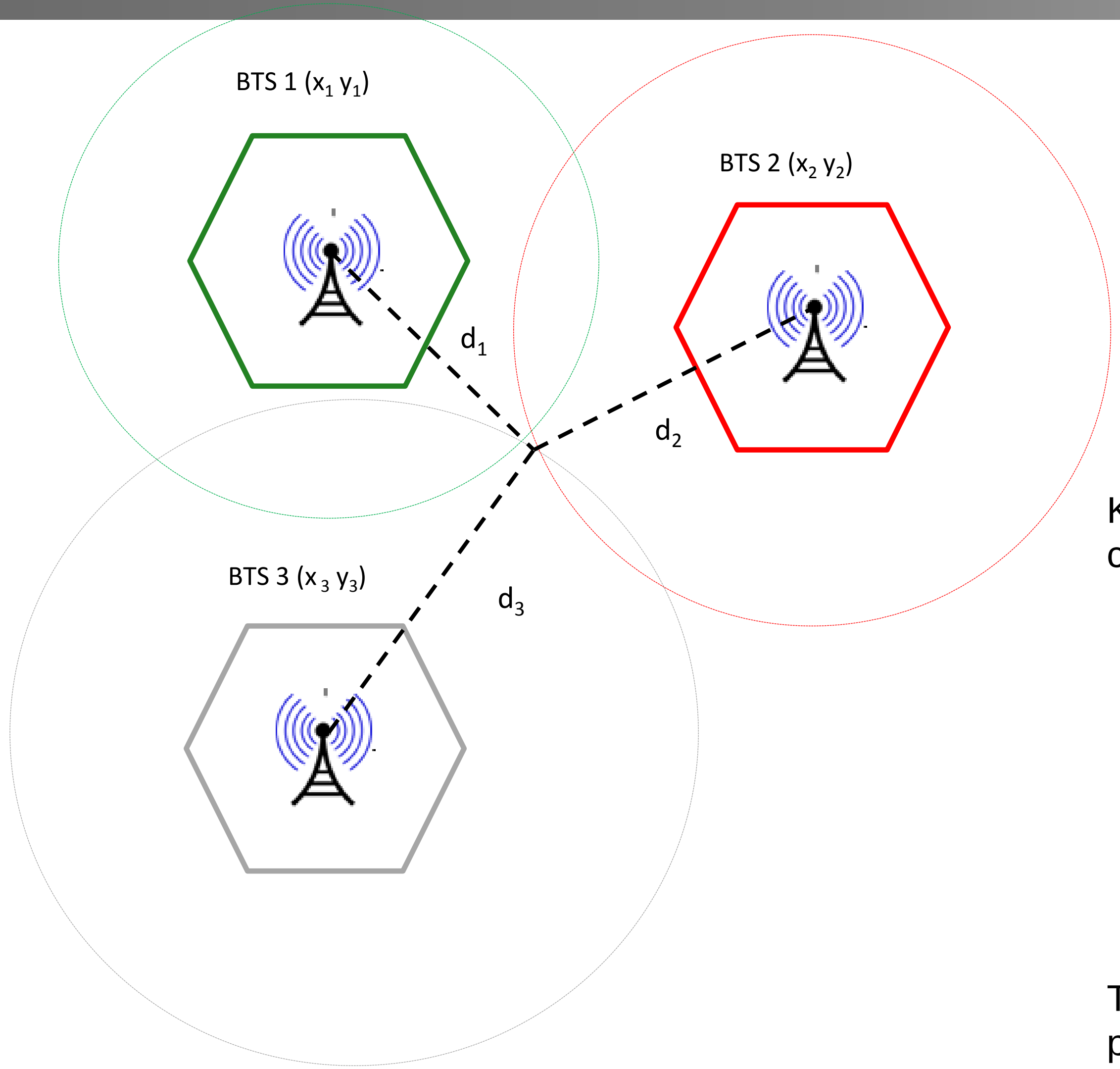
Signal at frequency f_0'

Moving end user at speed v shift frequency due to doppler effect then adding some time error

$$\Delta f = \frac{v}{c} . f_0$$

For TDD requirement time error from one cell to the next must be less than $\pm \mathbf{1.5}\mu s$ so as to keep same time reference

Why do we need time alignment?



Geo-Positionning

Knowing propagation speed and cells location one can assess distance by triangulation

$$\begin{cases} d_1 = c \times (t_1 - t_0) \\ d_2 = c \times (t_2 - t_0) \\ d_3 = c \times (t_3 - t_0) \end{cases}$$

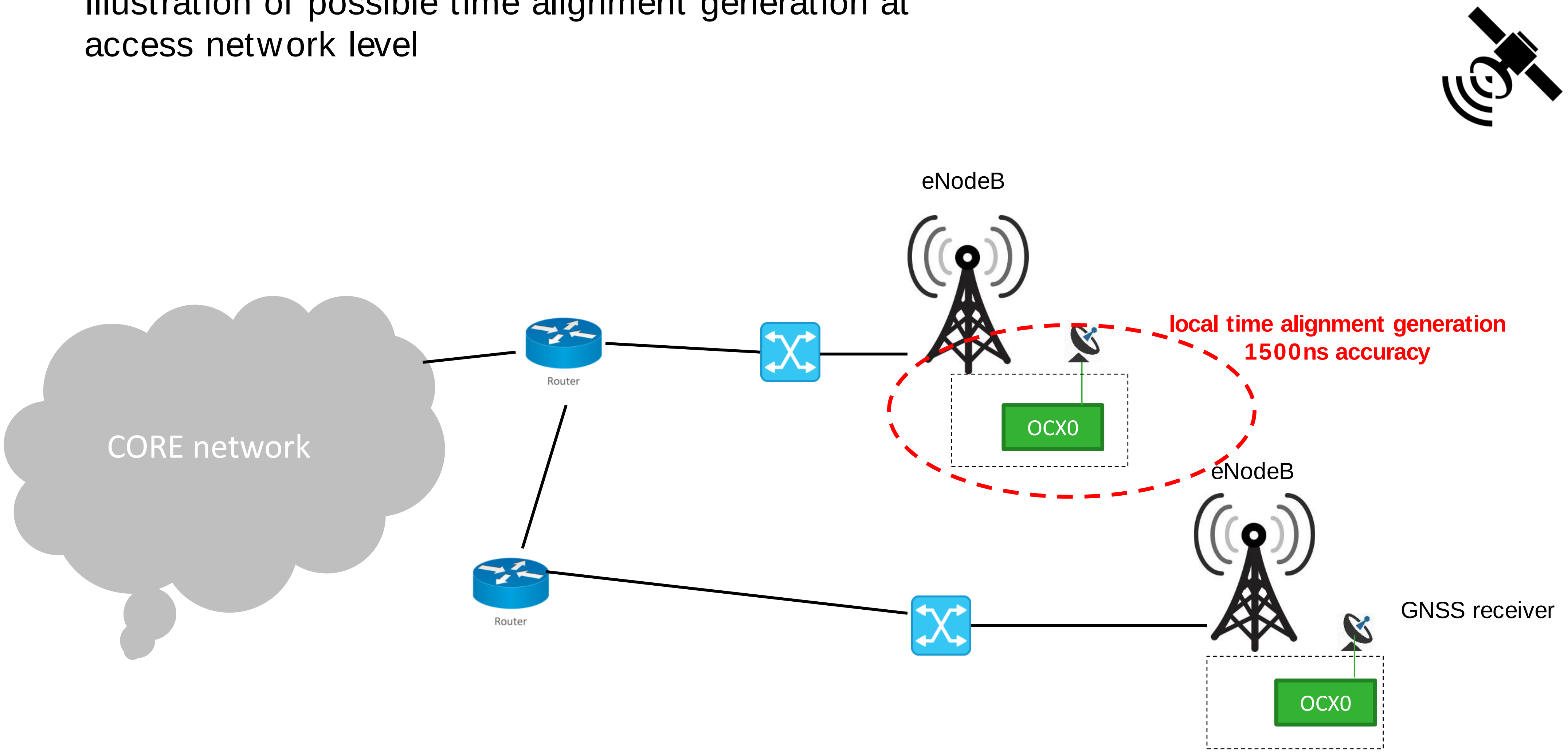
The more accurate the origin time t0 the better positionning accuracy

Comfortable accuracy can be achieved by having **100ns** time accuracy

How achieve time alignment in Network today?

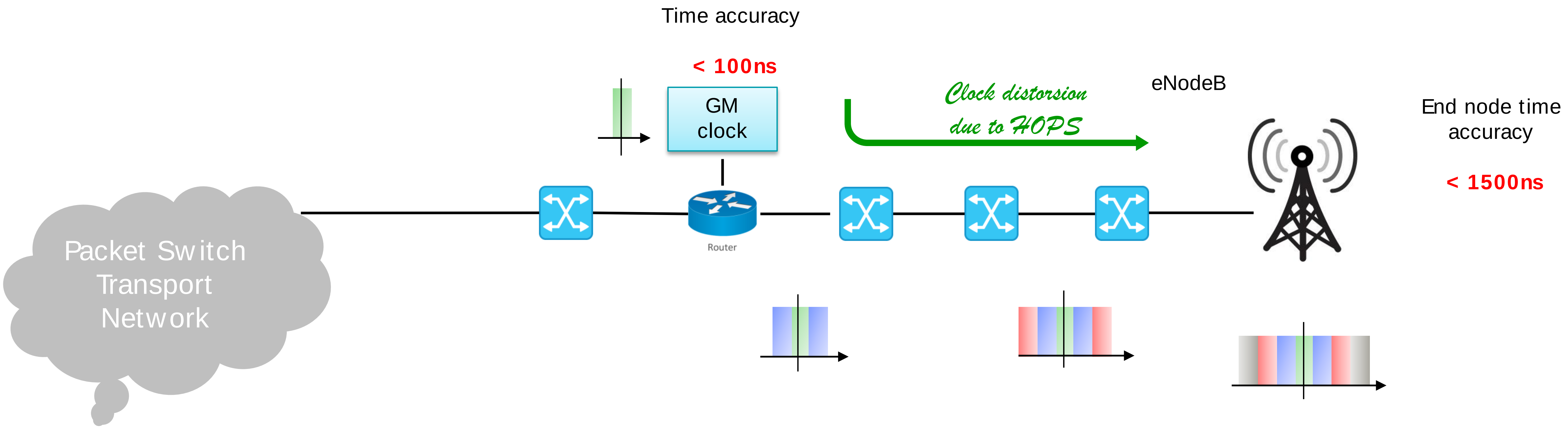
rakon

Illustration of possible time alignment generation at access network level



Possible evolution of network topology

Illustration of possible time alignment generation at access network level



Time alignment / time holdover

Main requirement for **time accuracy** are mainly

- 1500ns at eNodeB level

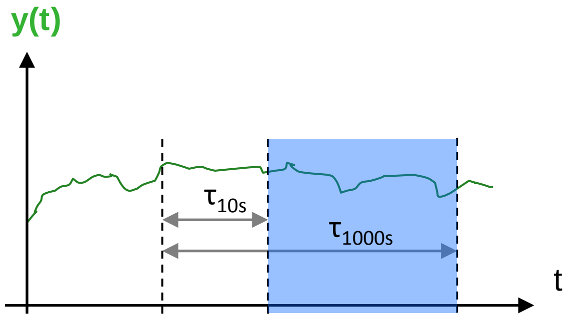
- 100ns at GrandMaster level

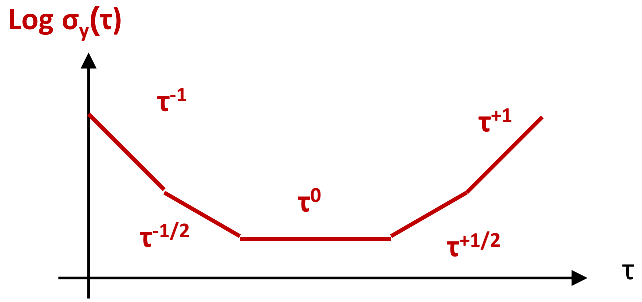
- Except primary clocks itself, there’s no way to generate a signal with accuracy over time without reference clocks.
- Challenge is then Time holdover capability and does translate to local oscillator specification

Time alignment / time holdover

Holdover performance being linked to oscillator performance, it is then convenient to approach different kind of clock stability through Allan Deviation ADEV

$$\sigma_y(\tau) = \sqrt{\frac{1}{2(M-1)} \sum_{i=1}^{M-1} (y_{i+1} - y_i)^2}$$





The Allan deviation gives an indication of how constant a clock frequency remains over an observation time τ

ADEV remains convergent, as it computes consecutive samples

Noise contribution can be identified through ADEV slope

Time alignment / time holdover

How to translate holdover requirement to frequency stability?

Time holdover x(t), or phase time is an accumulation of time error over observation time τ

It is simply computed by $x(t) = \int_0^{\tau} y(t)dt$ where y(t) is fractional frequency deviation (df/f)

Any change in frequency will lead to a time error x(t)

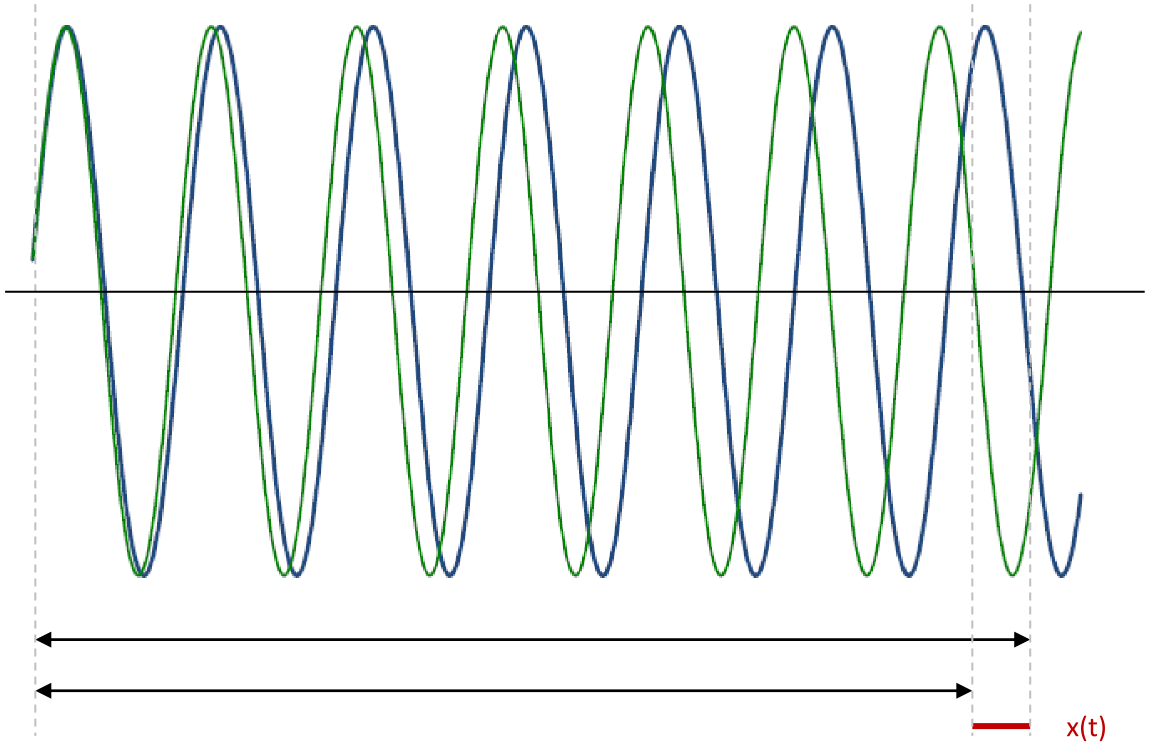
Considering initial phase error as well
as frequency initial error the global time error x(t)

$$x(t) = x_0 + y_0.t + \int_0^{\tau} y(t).dt$$

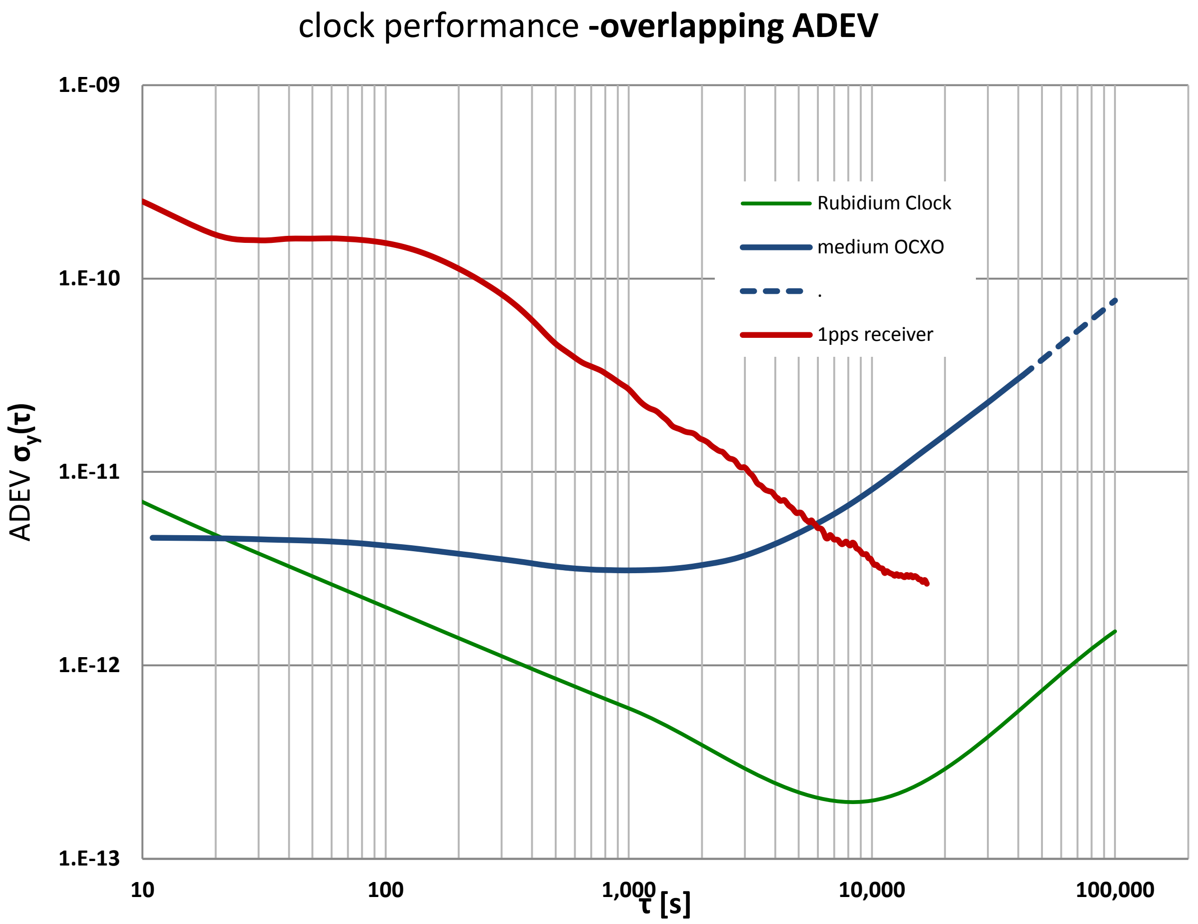
Initial phase offset

Initial frequency offset

frequency change over time



Clock signature -ADEV



Typical clock features with stabilized temperature :

Rubidium clock

are accurate but limited exhibits short term stability in the 1s range. In addition some ageing over time leads to frequency drift beyond 10 000s

OCXO

are stable and ADEV remains flat up to the 1000s but is affected by random walk frequency and by frequency drift beyond few 10 000s

GPS module receiver

are noisy in the 100s but become more accurate with longer integration time as it does eventually copy Caesium clock accuracy (GNSS)

Time holdover challenge

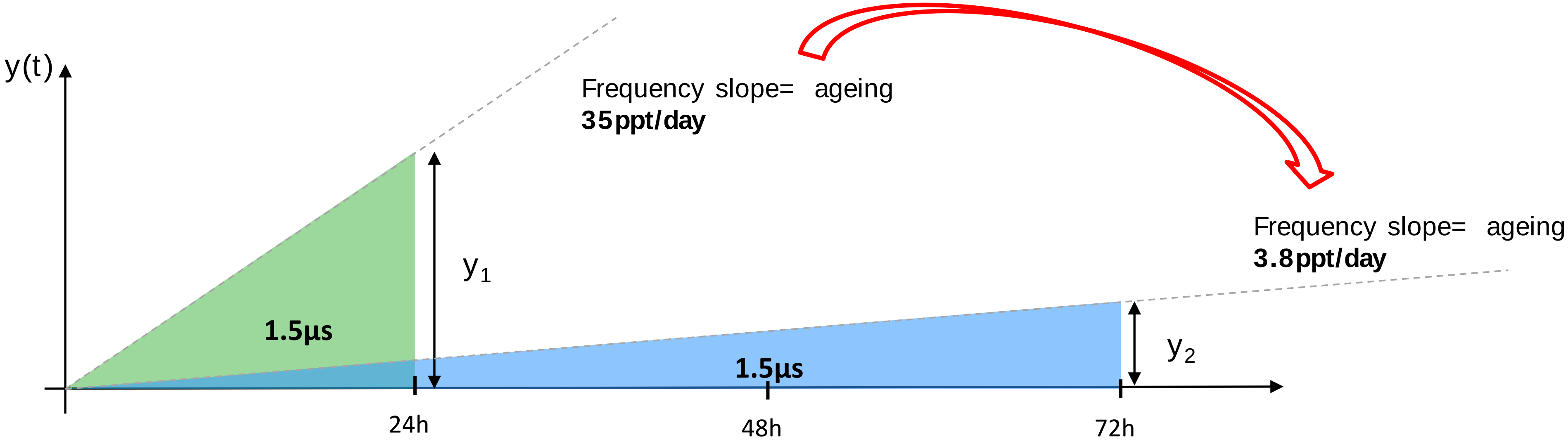
Before moving forward, some metrix…

As the holdover is the integral of y(t) over time, it is very convenient to represent trough area.

Both triangle have same area (holdover), as the blue one is 3 times longer its height is a third of the green one.

However the slope -frequency drift rate- is $3^2 = 9$ times lower

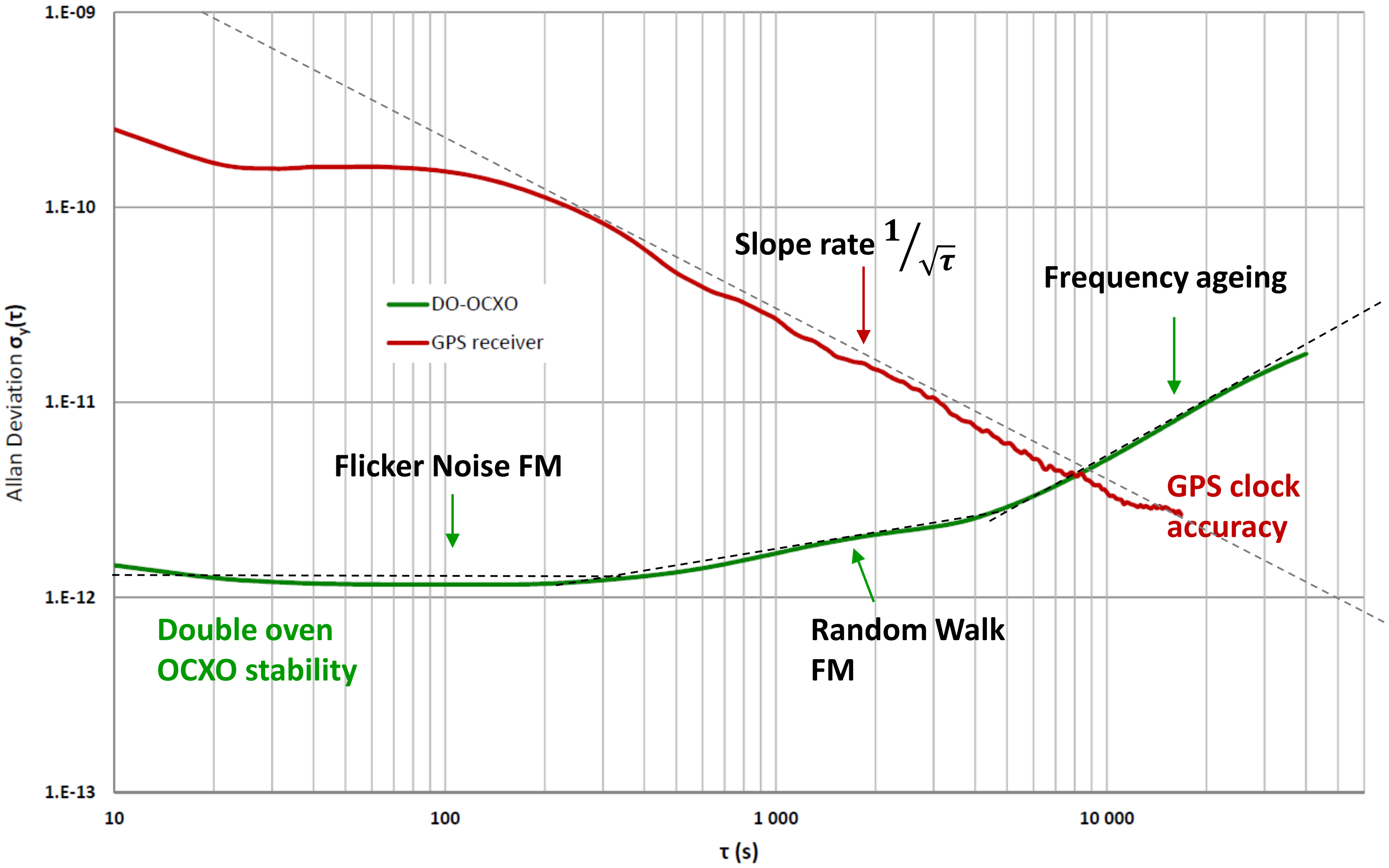
A **1.5µs** holdover is achieved with a frequency drift of **$3.5.10^{-11}$/day** for 24hours whereas the same performance requires a **$3.8.10^{-12}$/day** for a 72 hours time period



Technical challenge

So how to achieve time holdover capacity?

Find the « best of 2 worlds »: OCXO **stability** and Caesium clock **accuracy**



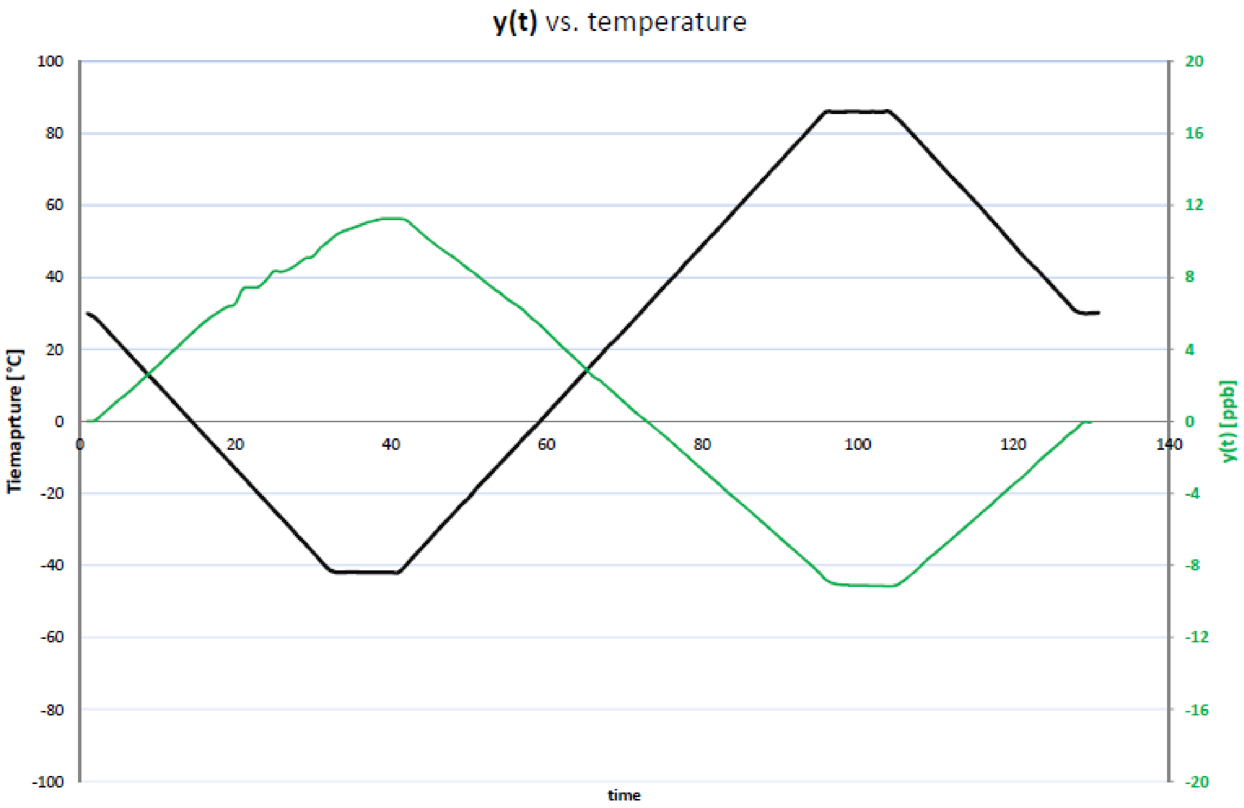
Note:

ADEV given at
room temperature

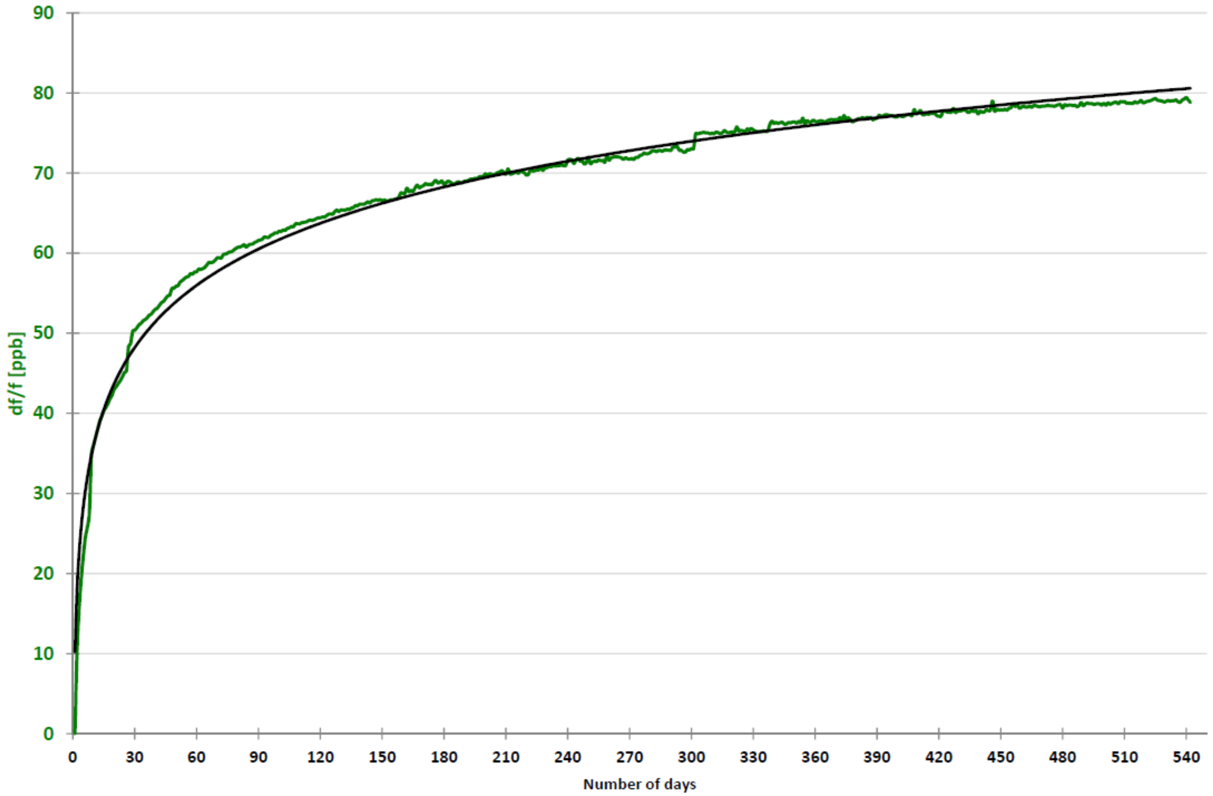
Technical limitation

- OCXO are Xtal based oscillator exhibiting highest quality factor Q. this bring significant advantage on their **short term stability**
- However OCXO are suffering of 2 main limitations:

Thermal sensitivity

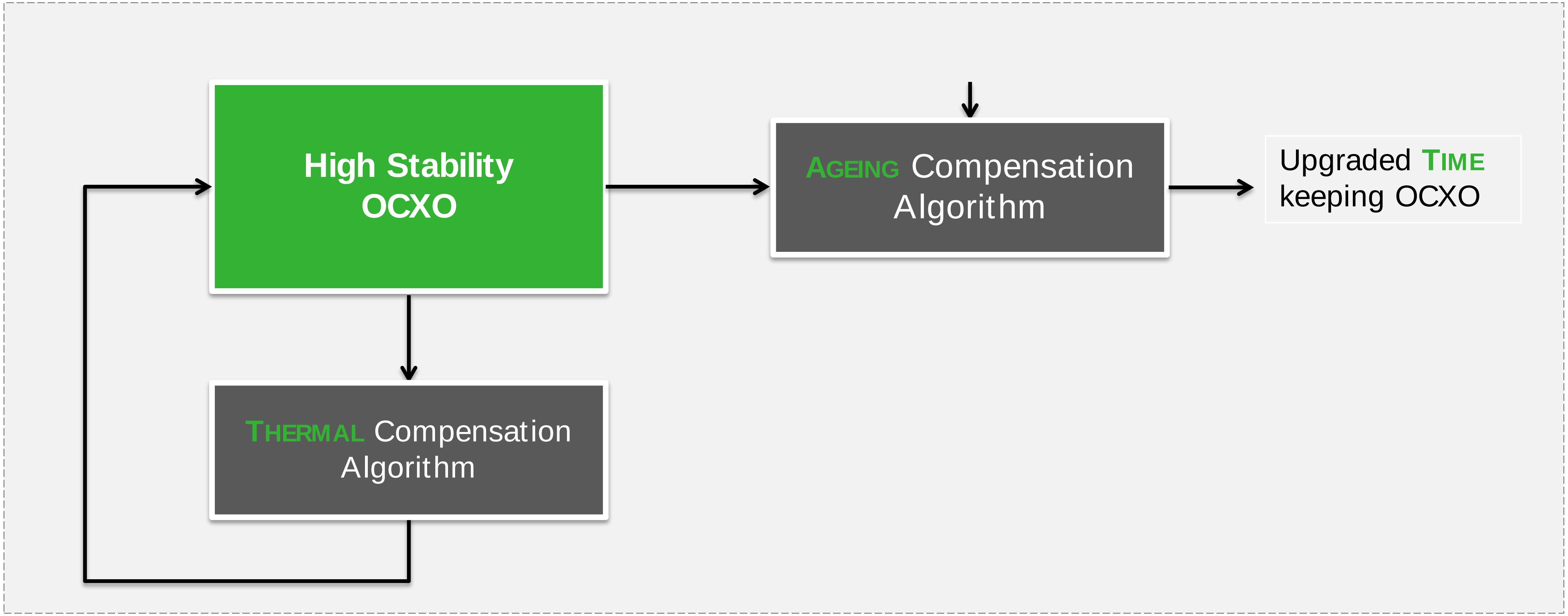


Frequency ageing



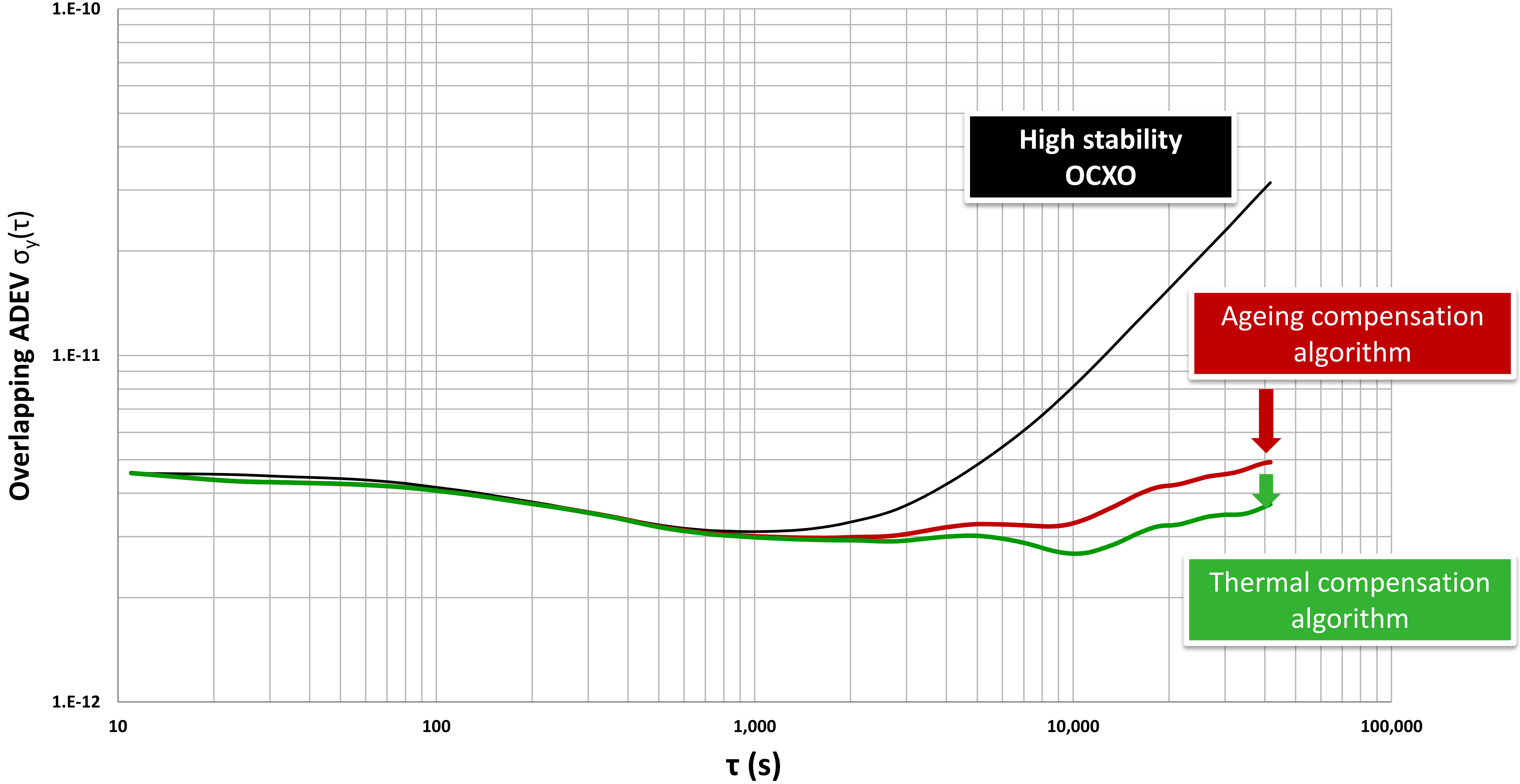
Technical limitation

- Overcome unwanted THERMAL and TIME effect



Frequency Instability Contributor ADEV Translation

rakon



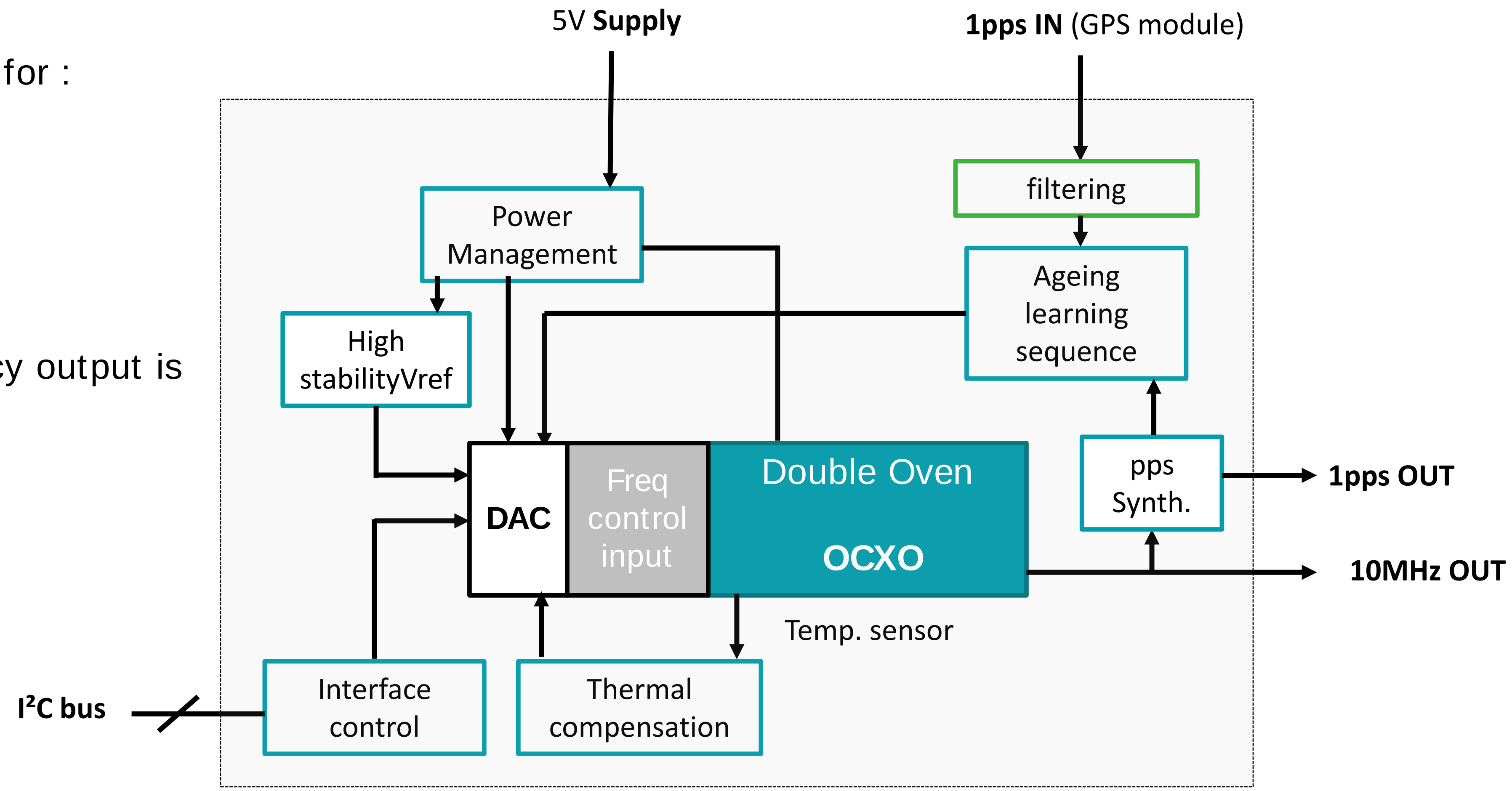
High-end module overview

Stand-alone Module

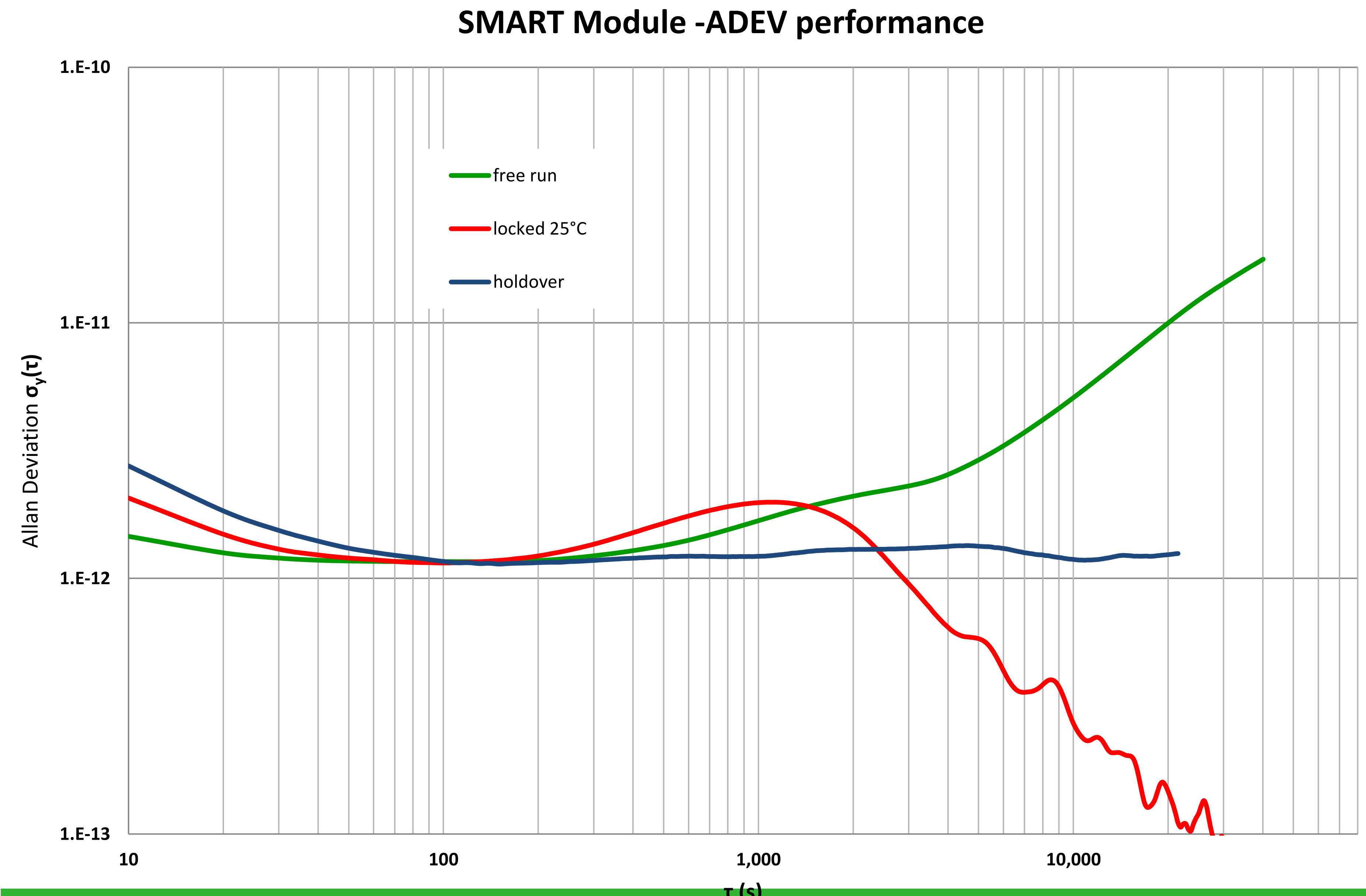
Including compensation for :

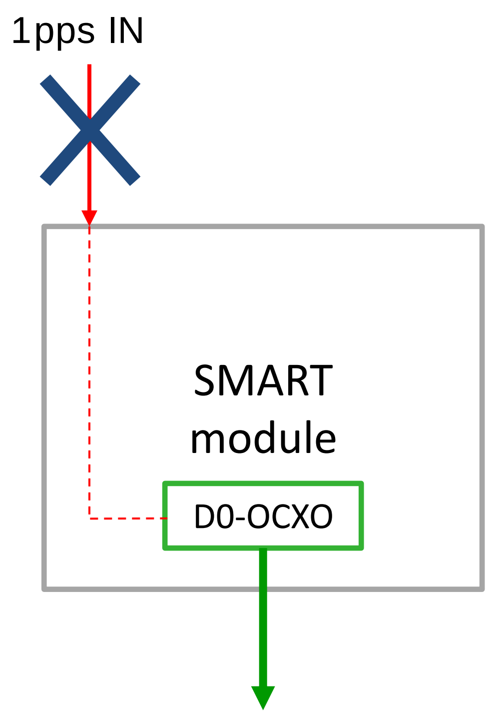
- Temperature
- Ageing
- Power supply

In addition, the frequency output is Digitally controlled



High-end module performance

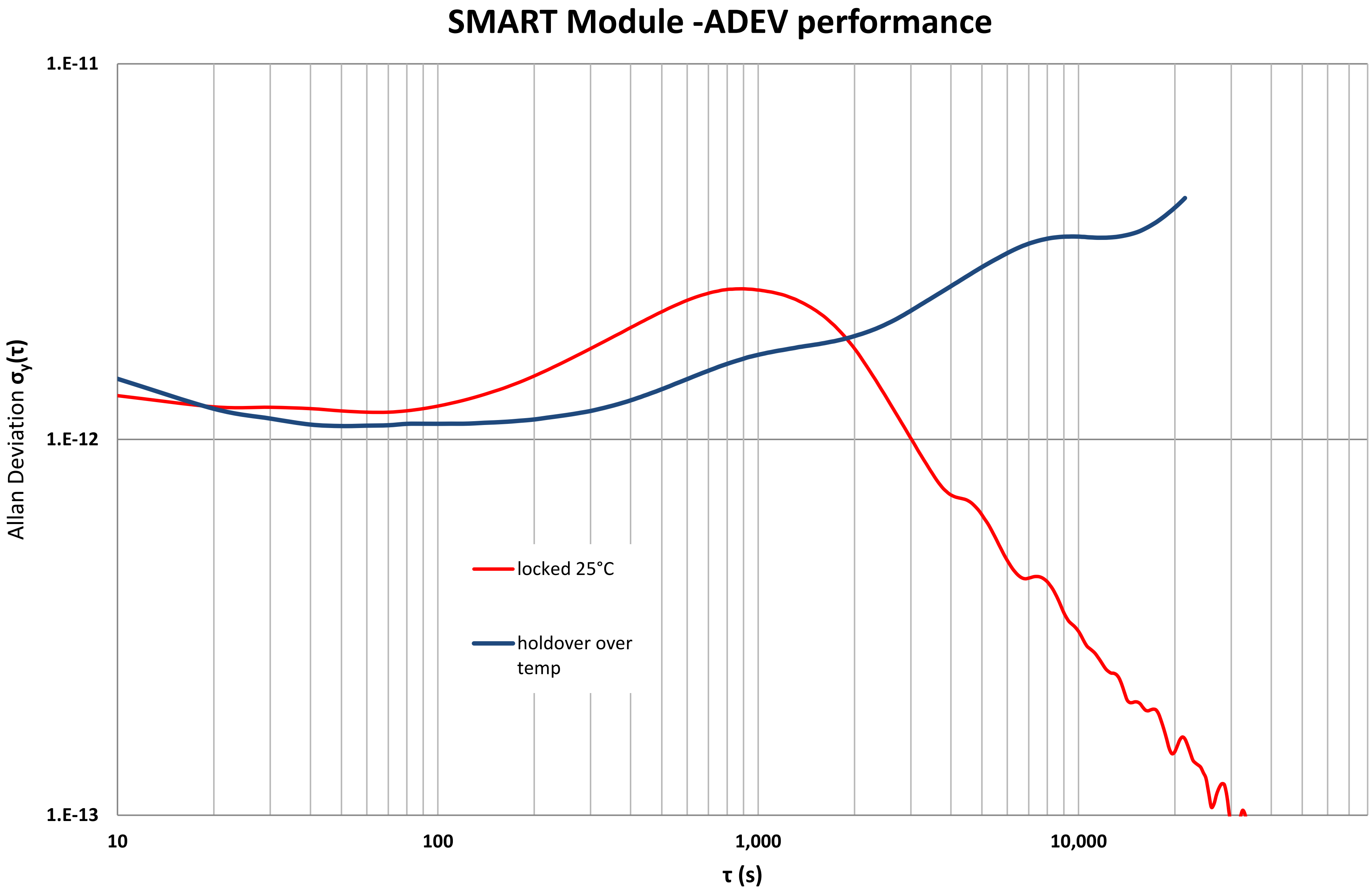




Note:

- 1pps locked and Holdover measured at 25° C

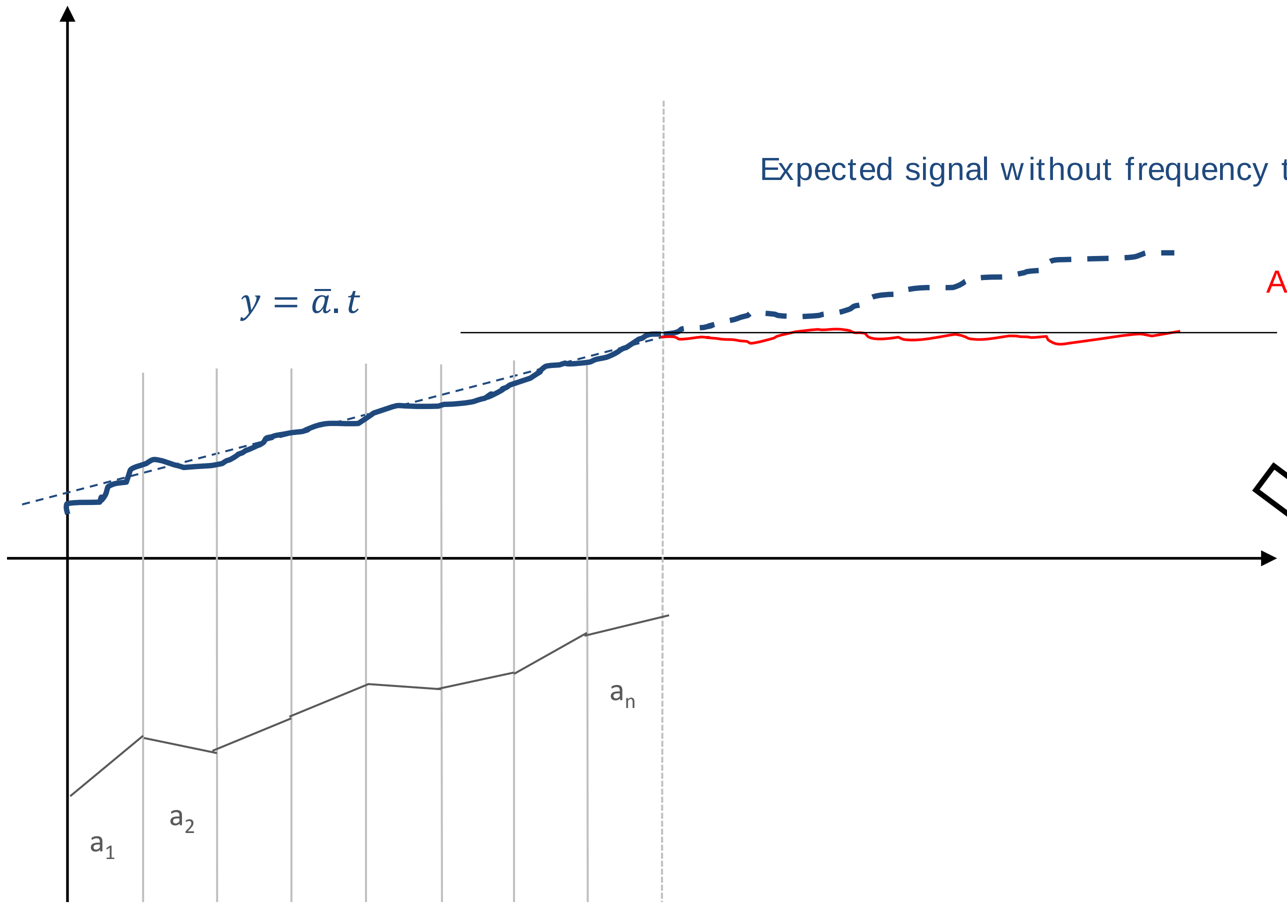
Temperature contribution

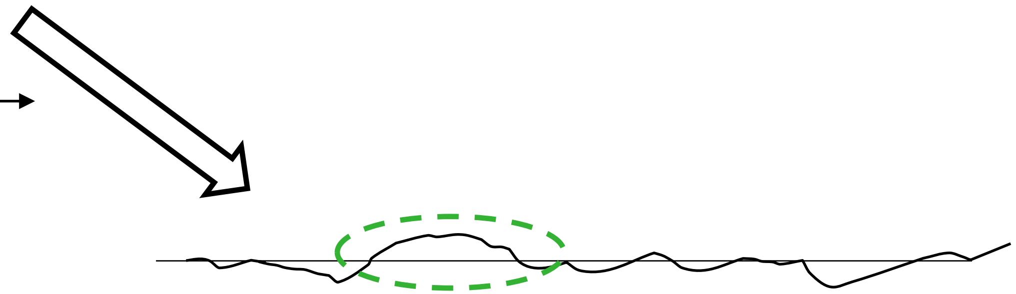


Holdover performance

Challenge is to extrapolate with accuracy the coming ageing sequence, based on consecutive slope sample

Multiple FIR is applied



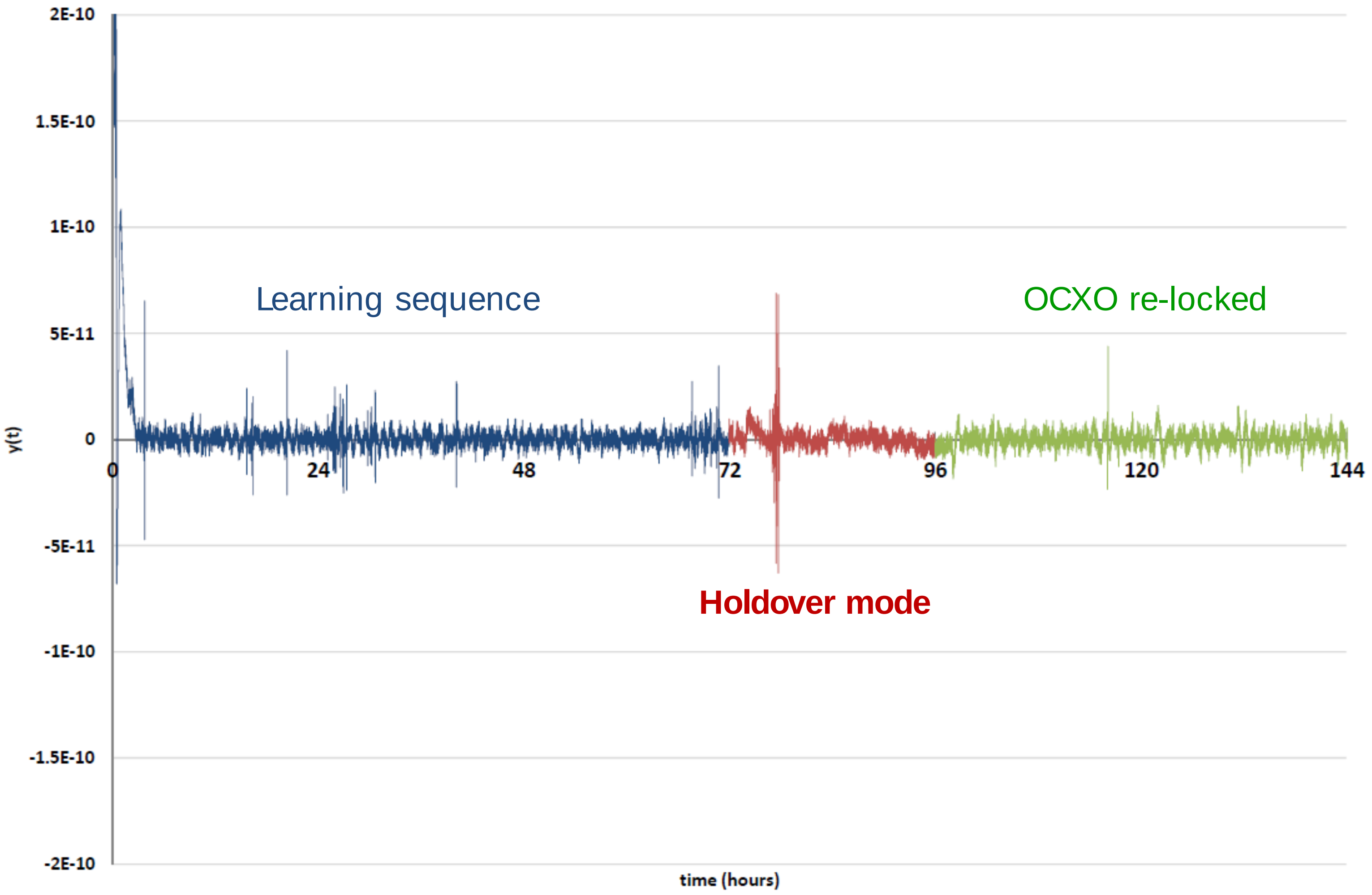


The non predictable part of the signal does condition phase accumulation error

Holdover performance

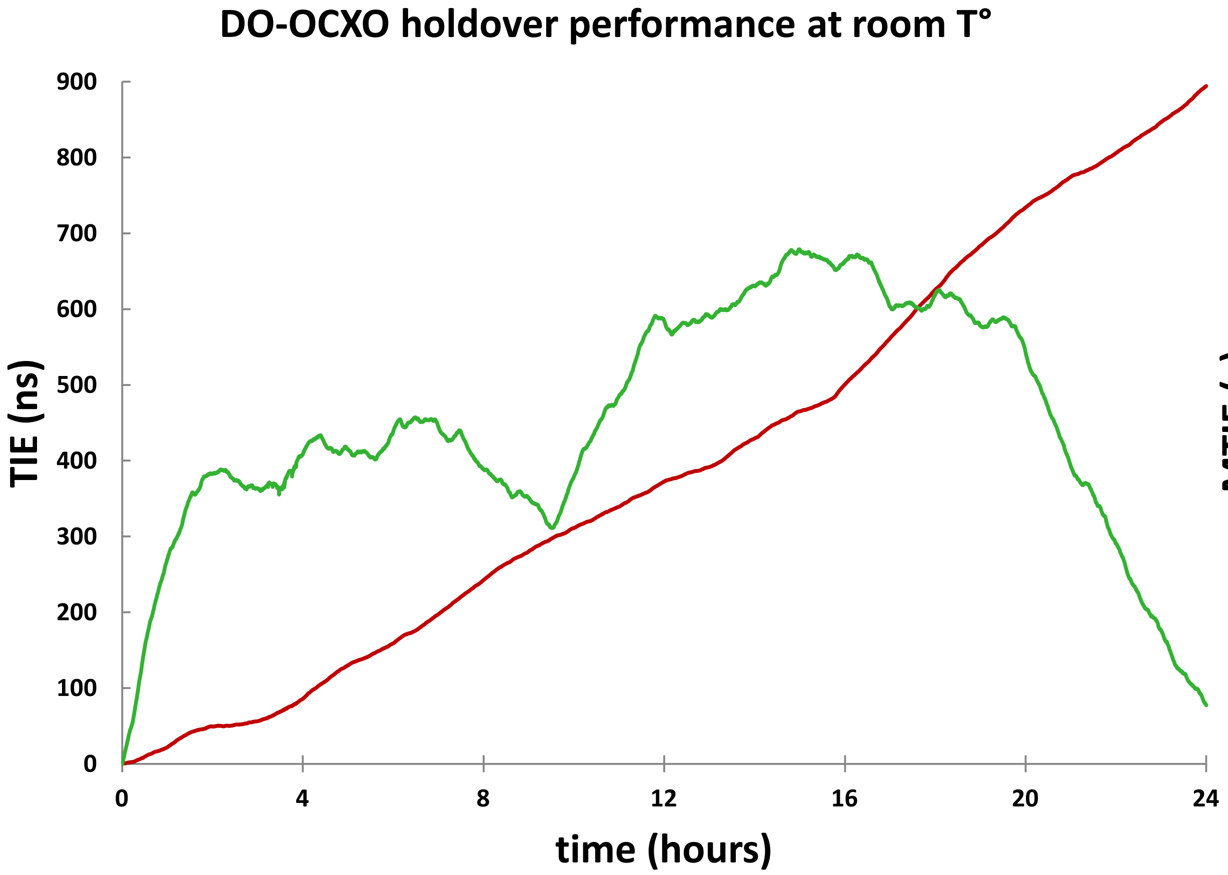
A prior « learning sequence » is required so as to evaluate ageing trend over the past hours

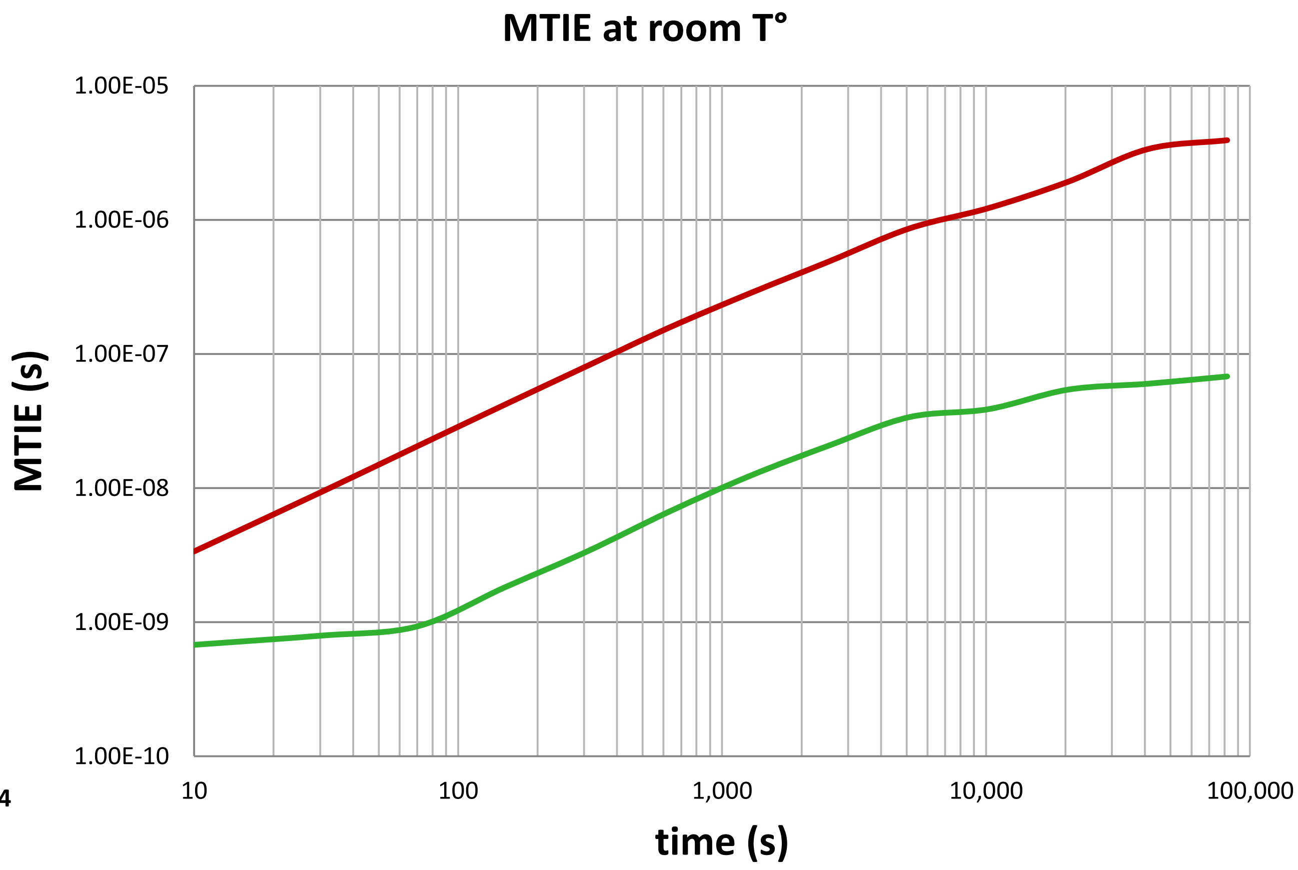
When disciplining signal is lost, the ageing is extrapolated based on the averaged ageing trend



Holdover performance @room temp

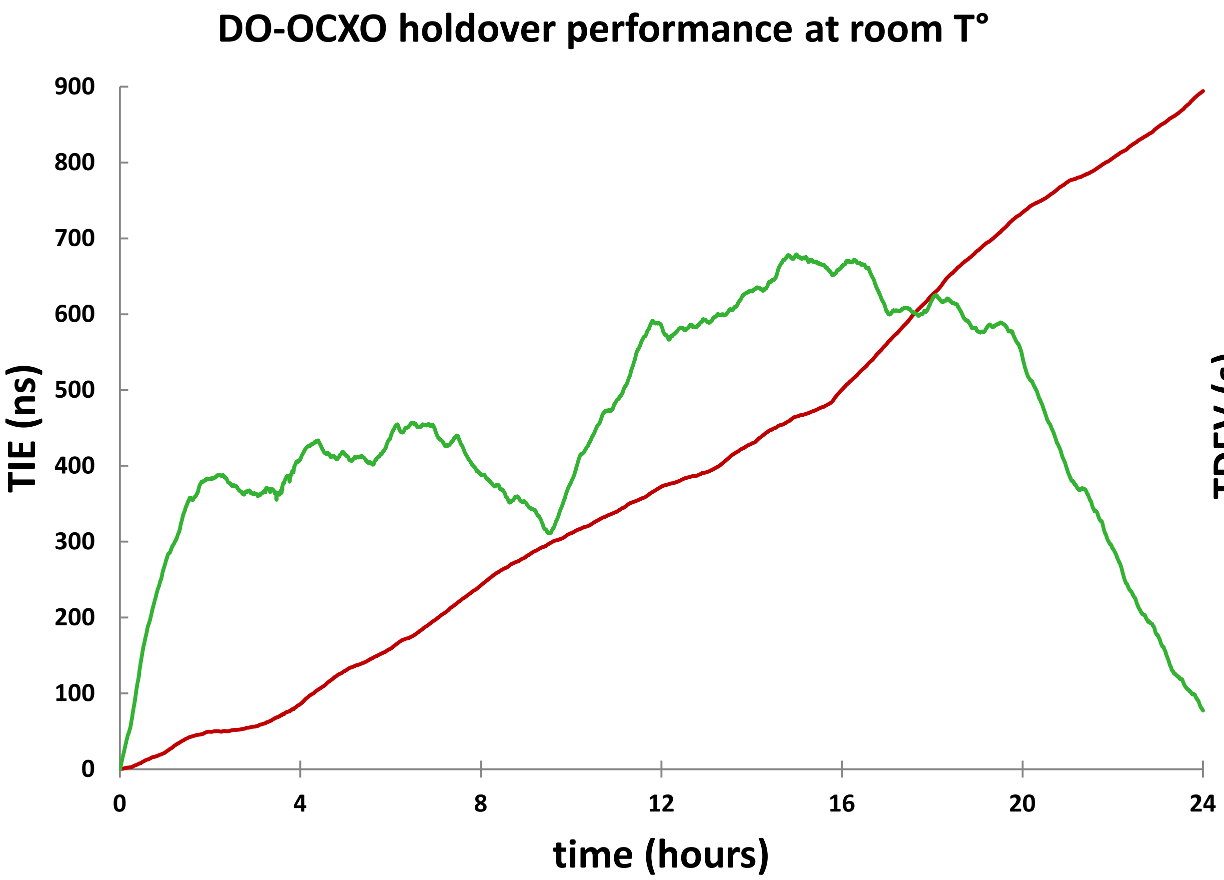
Module performance are mainly linked to ageing predictability over time
Two parts performance are represented (part**1** & part**2**)

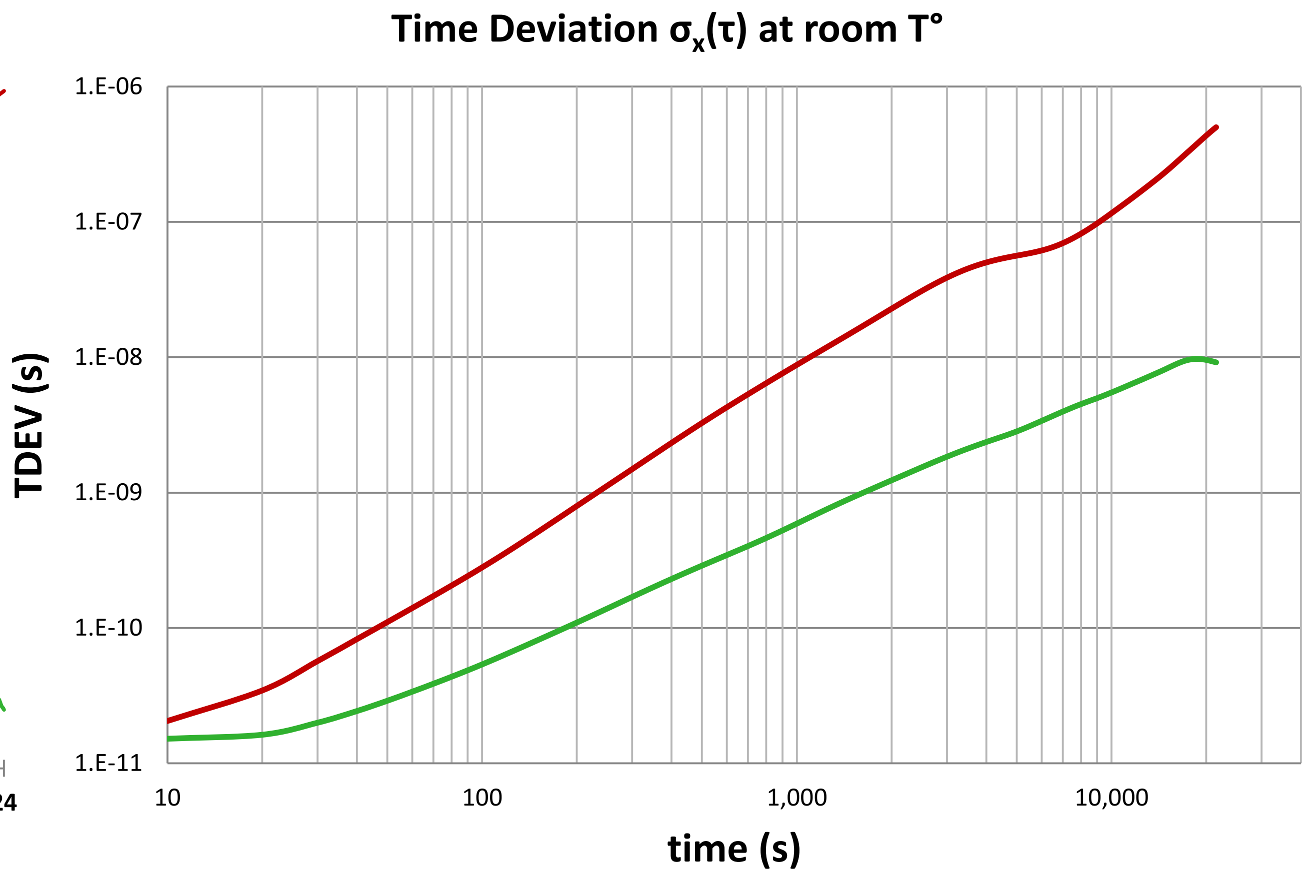




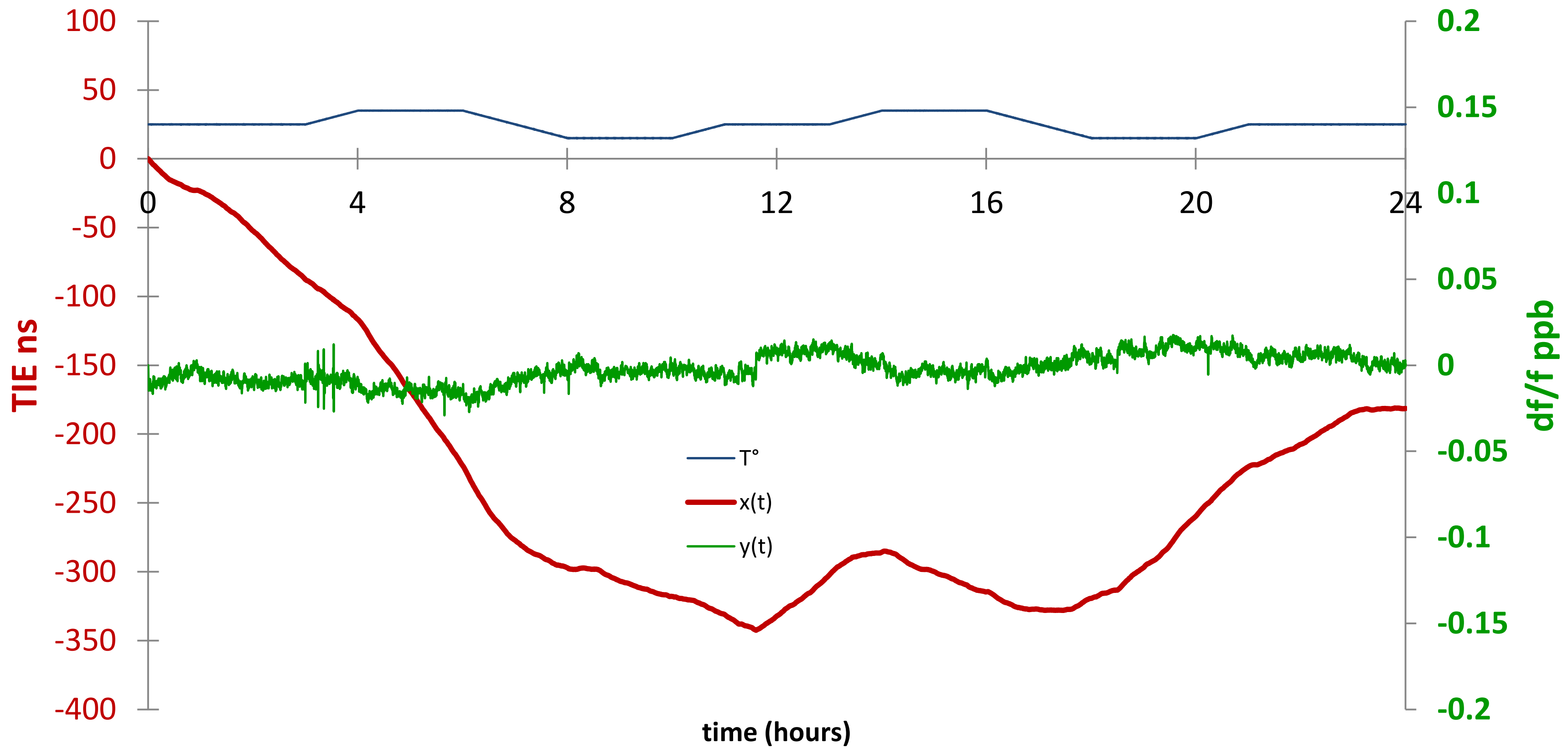
Holdover performance @room temp

rakon





Holdover performance over temp



Conclusion

OCXO Module are now able to combine short and mid term stability so as to address tight specification

1500ns over **48hours**

100ns over **4hours**

Continuous improvement in Xtal design will extend tomorrow holdover capabilities. As global stability becomes highly critical, component contributions are such, regulation and control must be embedded in module.

Meeting such tight time keeping specification does require an accurate OCXO ageing predictability, more than ever Xtal design and manufacturing expertise remains then key factor to achieve future performances.

Thank you!