Improving Equipment Clocks

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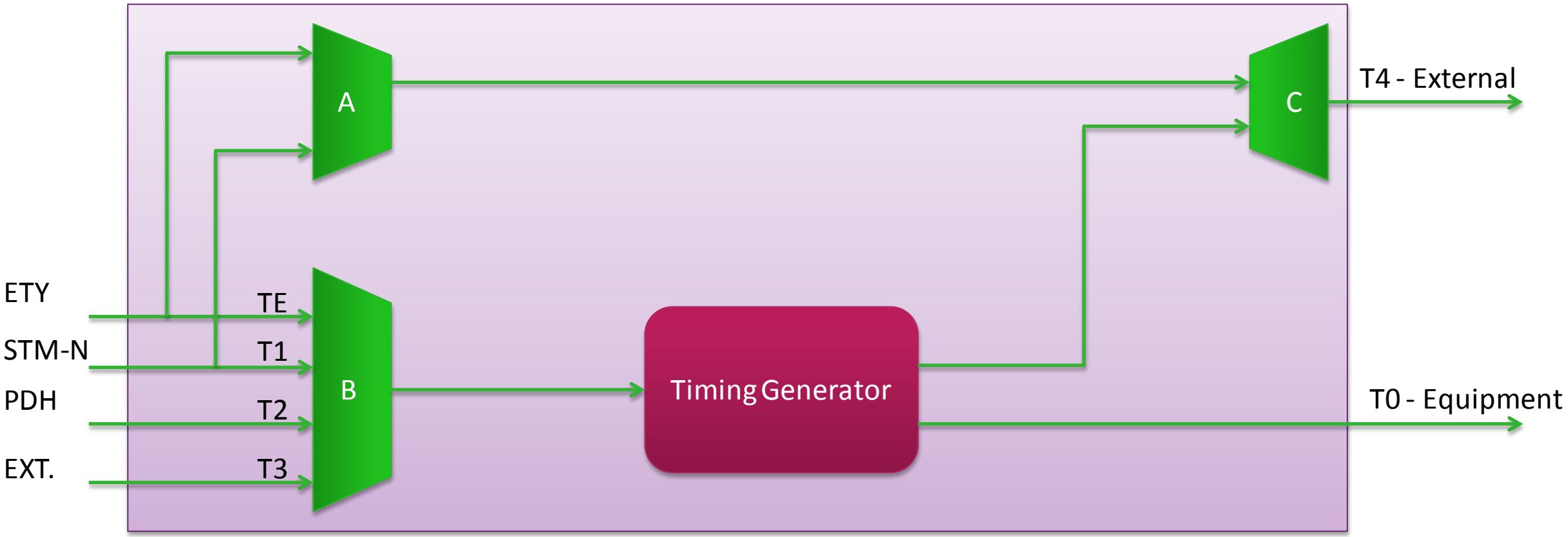
1 Agenda

- Equipment Clocks
- Overall clock improvements
- Effects – Reference Clocks, Servo, System & Interaction
- Improvement possibilities

Equipment Clock blocks



G.8264-Y.1364 (14) _FA.2

Equipment Clocks

SDH

- G.813
  - SDH Slave Equipment Clock

Ethernet

- G.8262
  - Ethernet Equipment Clock

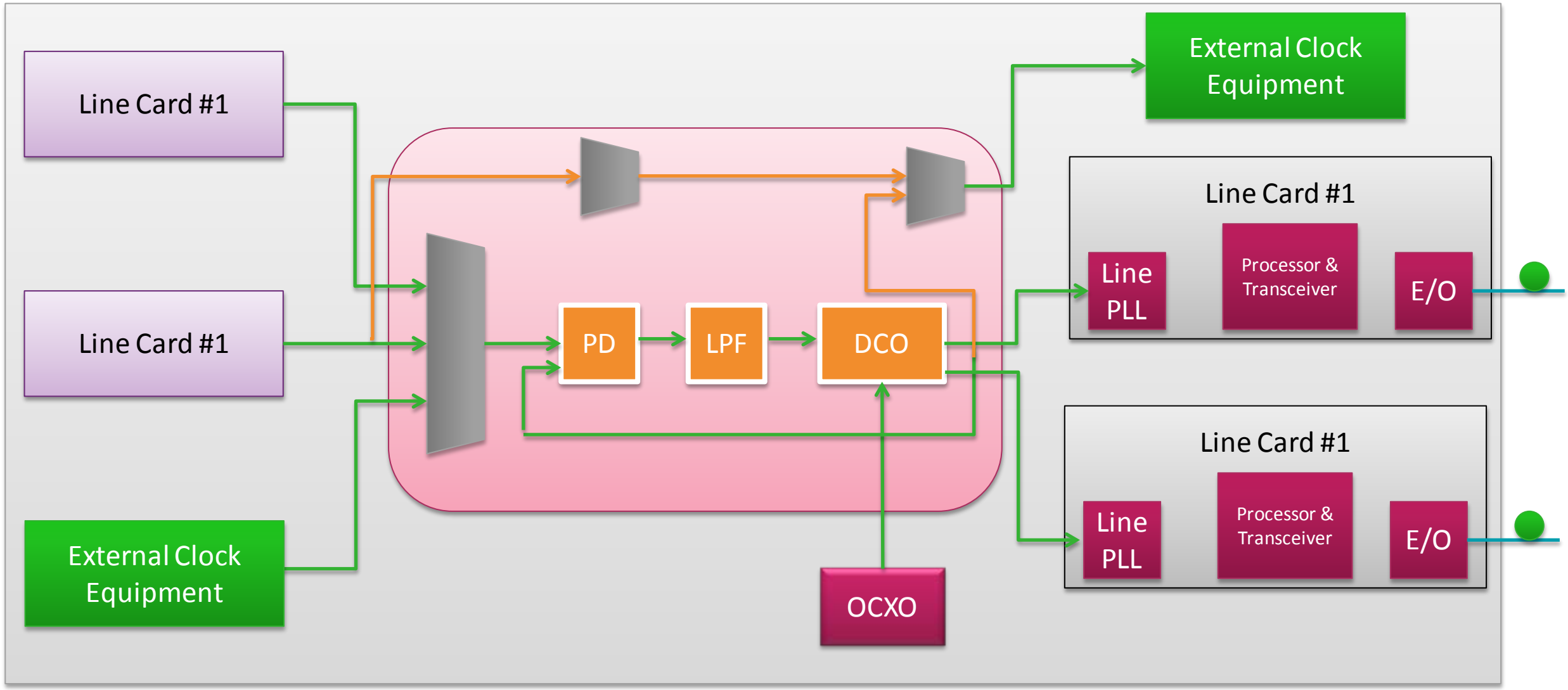
Option 1 – Based on E1 Hierarchy of Networks (Europe and Asia)
Option 2 – Based on T1 Hierarchy of Networks (North America)

G.8263 defines Packet Equipment Clock - Frequency

Improvement in Reference Clocks & Servos

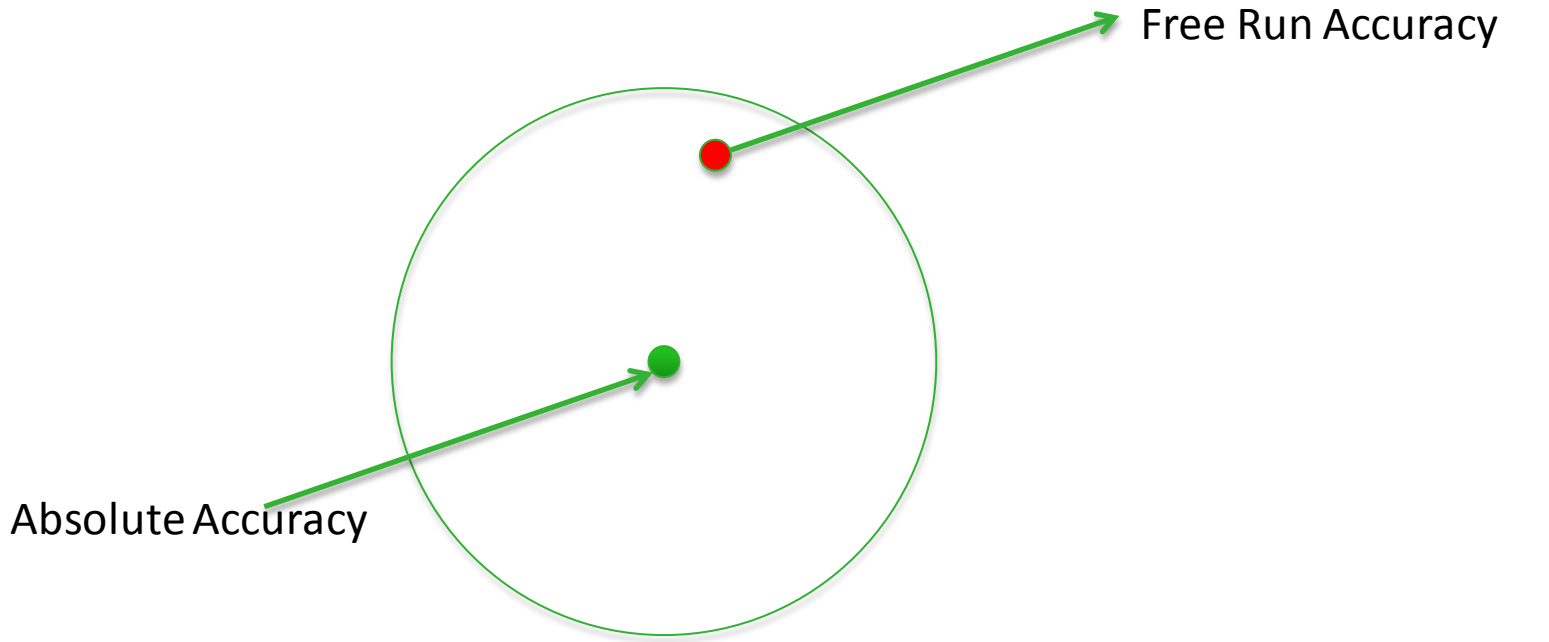
Technology Improvements bring superior performance at the same cost

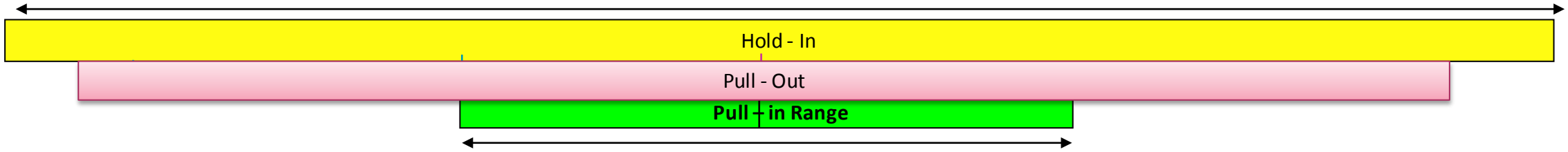
General Clock Architectures



Basic Features – Improvements?

- **Free Run Accuracy**
- **Pull – in Range**
- **Pull – Out Range**
- **Hold – In Range**





Noise – Jitter – Improvements?

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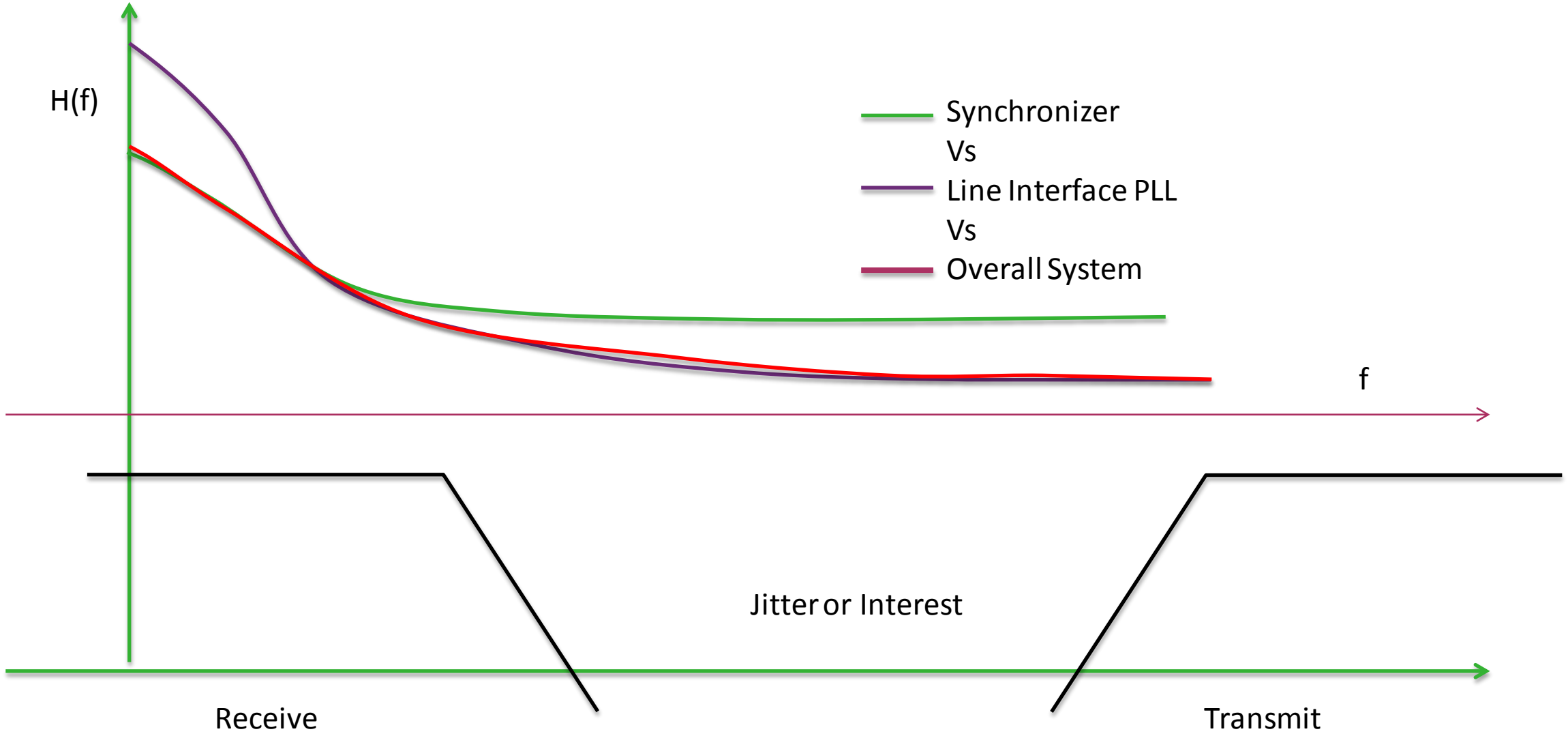
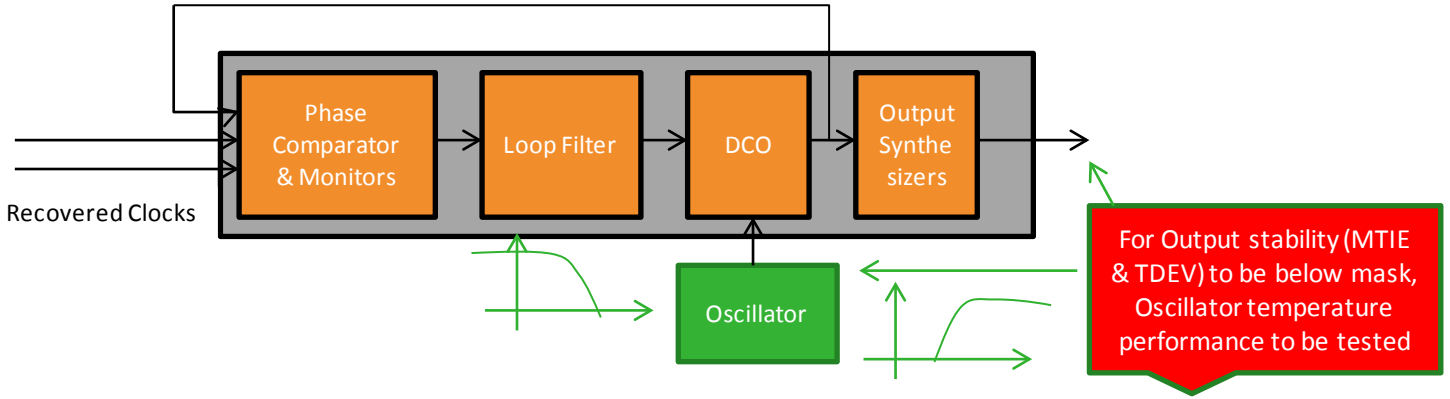
Generation



Wander Generation



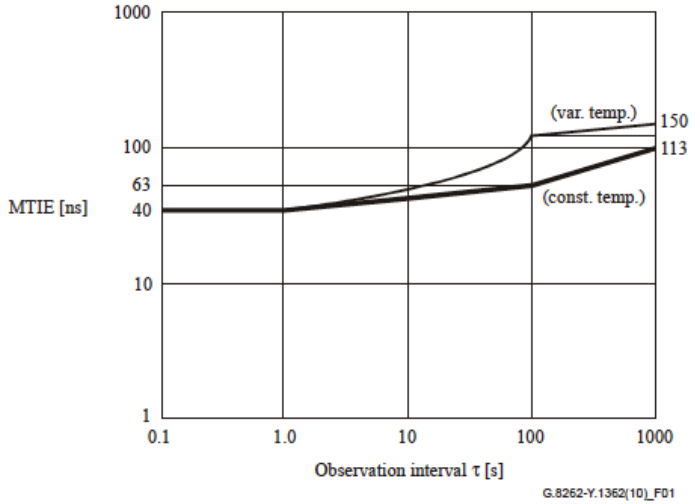
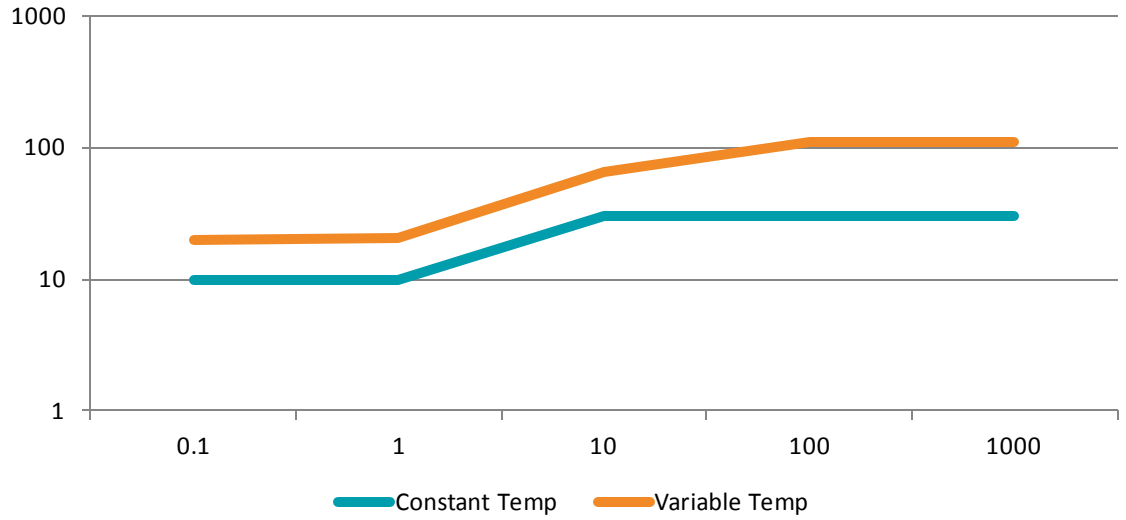


Figure 1 – Wander generation (MTIE) for EEC-Option 1

MTIE limit (ns)	Observation Interval τ (ns)
10	0.1<τ≤1
$10\tau^{0.1}$	1<τ≤100
$6.3\tau^{0.2}$	100<τ≤1000

Temeperatuer effects

0.5τ	τ≤100
50	τ>100



Noise Transfer – Improvements?

- **Loop bandwidth Recommendations**
  - 1-10 Hz for Option 1
  - 0.1Hz for Option 2
  - ~ 1mHz for G.8263
  - 0.05-0.1Hz for G.8273.2/G.8273.2

- **Harmonize to Packet Clocks**
  - 0.05Hz to 0.1Hz for all applications

Short Term phase transient response

Reference Switching or Input interruptions

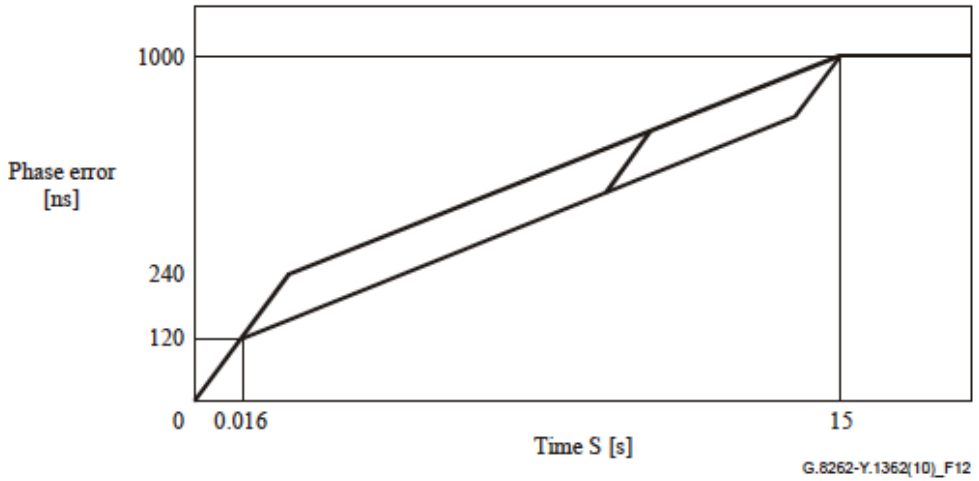
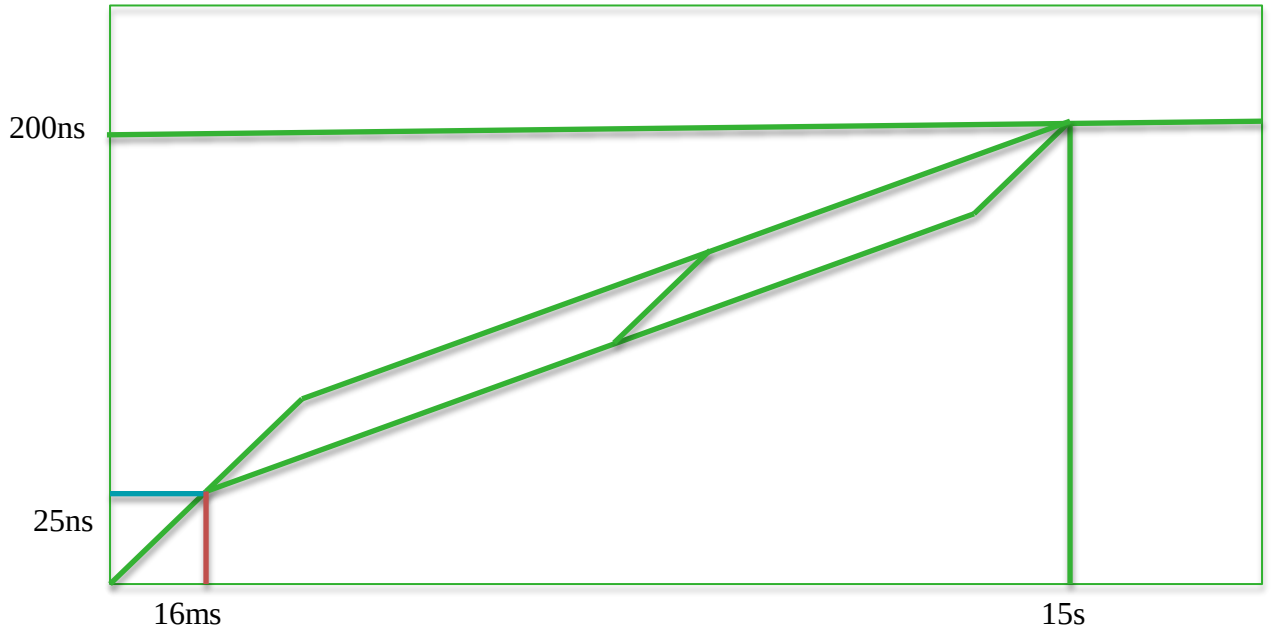


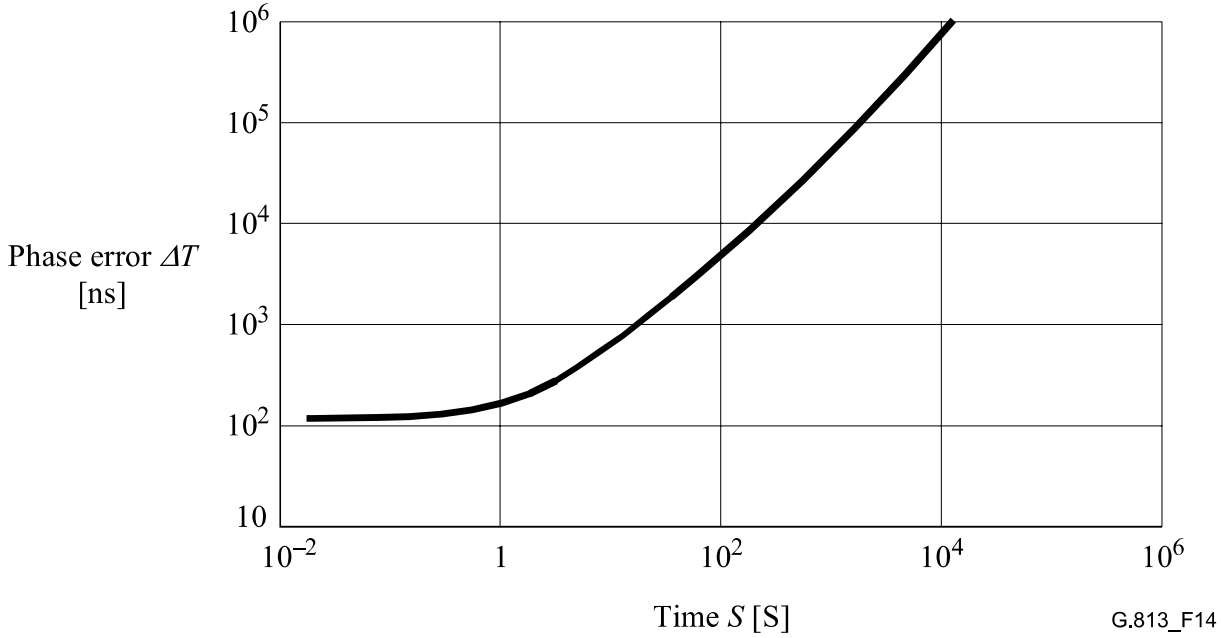
Figure 12 – Maximum phase transient at the output due to reference switching for EEC-Option 1



Entry to holdover – 25ns Max each for two possible transitions
Max phase slope for entry to holdover – 1.6ppm
>16ms, upto 15 seconds – 10ppb phase error

Max phase error – 200ns

Long Term Holdover



$$\Delta T(S) = \{(a_1 + a_2)\, S + 0.5\, b\, S^2 + c\} \quad [\text{ns}]$$

where:

a_1 = 50 ns/s (see Note 1);

a_2 = 2000 ns/s (see Note 2);

b = 1.16×10^{-4} ns/s^2 (see Note 3);

c = 120 ns (see Note 4).

Long Term Holdover

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Item	Description	Units	Option 1	Option 2	Proposal
S	Duration	Seconds	S>15	TBD	1 year
a1	Initial Accuracy	ns/s	50	50	1
a2	Temperature Effects	Ns/s	2000	300	100
b	Oscillator ageing	ns/s2	1.16E-04 (10ppb/day)	4.63E-04	1.16E-04 (10ppb/day)
c	Entry/Exit phase error	ns	120	1000	25
d	Drift	ns/s2	-	4.63E-04	-

Critical Improvements

- **Temperature stability**
  - Improved algorithms and thermal designs
  - Cost impact
- **Temperature slope**
  - Quality crystals, improved test equipment
- **Ageing**
  - Improved crystals
- **PLLs with fine resolution controls**
  - Output phase movements <1ppt
- **Integration**
  - Digital interfaces, Smart compensation

Summary

- **With advancement in Oscillator and PLL technologies, significant performance improvement on equipment clocks possible**
- **Significant performance Improvements are possible on**
  - Wander generation
  - Short term phase transient response
  - Long term holdover
  - Phase response to input signal interruptions
  - Phase discontinuity

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Thank You