Testing Challenges Arising in Packet-Based Clocks

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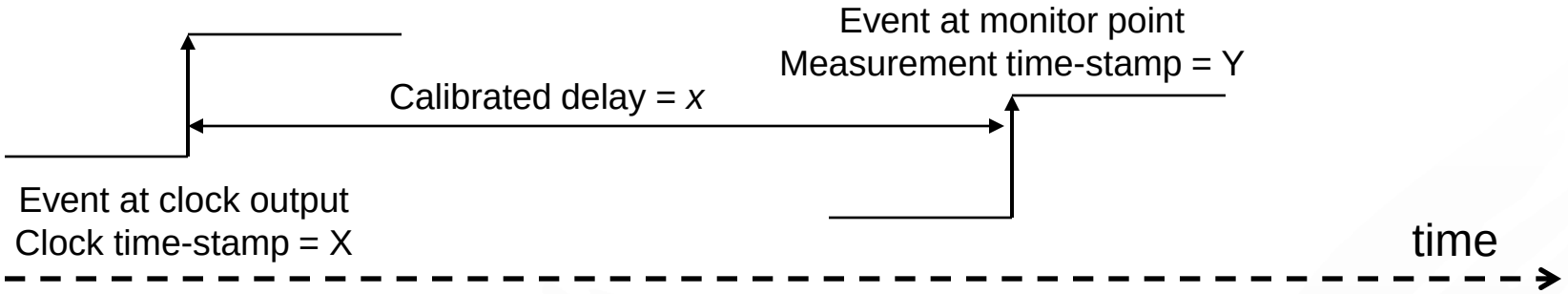
Agenda

- Time Error
  - Definition
  - Standards-defined limits
  - Time Error contribution PTP devices
- Testing Time Error contribution of devices
  - Boundary Clocks
  - Transparent Clocks
- Concluding Remarks

Defining Time Error



- Time Error: TE(n) = (X(n) + *x* – Y(n))
- Time Error deconstructed into *constant time error* (“DC component”, “static offset”) and *dynamic time error* (“AC component”, “TIE”)
  - Constant Time Error: measure of ***accuracy***
  - Dynamic Time Error: represents ***stability***
- The measurement accuracy of the tester must be significantly better than the requirement for time-stamp accuracy.

Time Error Limits

- IEEE C37 238 (PTP in Power Systems) defines limits:
  - Network consists of 16 hops – TE contribution of each hop adds up to total TE budget
  - Total Time Error (“TimeInaccuracy”) of whole network allowed: **+/- 1µs**
    - Grandmaster: **200ns**
    - Each Transparent Clock: **50ns**
- Other Standards Developing

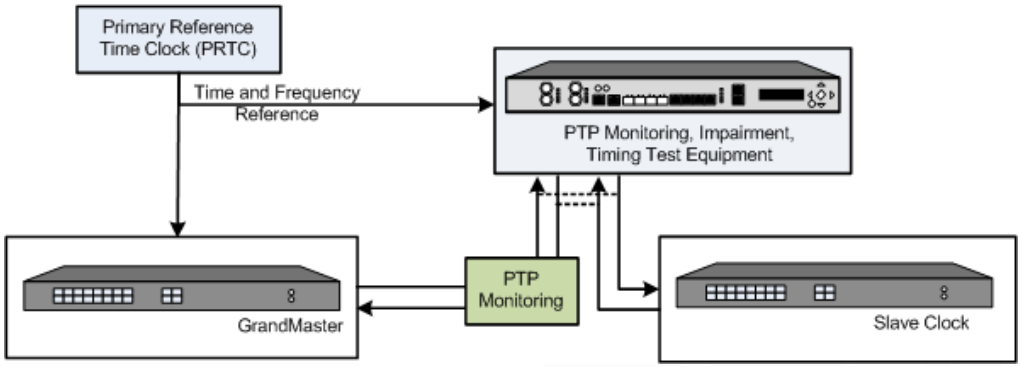
Time Error: Master

- GPS
  - ToD + 1PPS: +/- 50ns to UTC typical
- Grand Master Clock
  - PTP timestamp + 1PPS: +/- 50ns to UTC typical
    - 200ns TE limit (“TimeInaccuracy”) suggested by IEEE C37 238
  - Time Error evident
    - Difference between 1PPS and PTP timestamp time, constant time error + dynamic time error
    - Packet-to-packet timestamp variability (dynamic time error)
    - Accumulation of constant dynamic time error of timestamps
- Time Error of GM Clock contributes to overall time error in the network, must be measured

G.8273 Testing Annexes (A&B)

- Annex A (What to measure)
  - A.1: Introduction
  - A.1.1: Master Port Timestamps
  - A.1.2: Master Port Time Xfer
  - A.2: GM
  - A.3: BC
  - A.4: TC
  - A.5: Slave
- Annex B (How to measure)
  - B.1: Overview
  - B.1.1: Active Method
  - B.1.2: Passive Method
  - B.2: GM
  - B.3: BC
  - B.4: TC
  - B.5: Slave

Testing Master Ports (G.8273 Annex A&B)



Passive measurement set up for testing a Master Port (e.g.GM):

a. Time-stamp accuracy
b. Time-transfer accuracy

- Monitor device “sniffs” PTP packets and time-stamps the time of passage
- Cable delays between monitor device and SUT must be known/calibrated
- Time-stamp accuracy of “T1” (*sync_message or follow_up*) measured directly
- For measuring accuracy of “T4”, the time-stamp of *delay_request* by master clock is available in *delay_response*
- *Packet Inspection* required for extracting time-stamp values

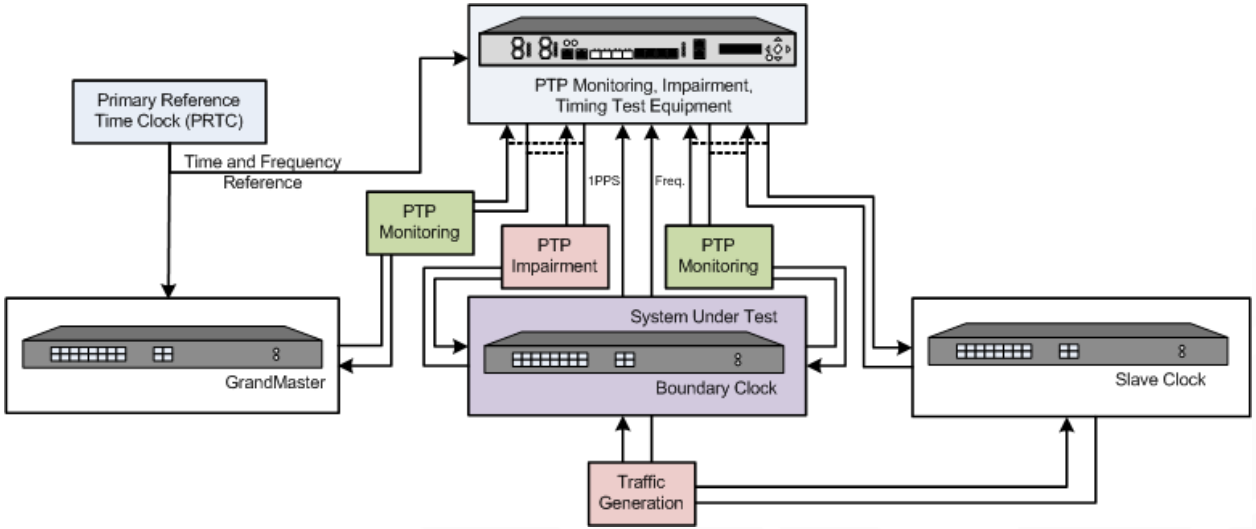
Time Error: Boundary Clocks

- Boundary Clock
  - PTP timestamp + 1PPS: accuracy unknown!
    - Limits still being defined
  - Error of PTP timestamps
    - Accuracy of time recovery depends on accuracy of incoming PTP timestamps
      - GM Dynamic Time Error + PDV from the network
      - Constant time error + rate adaptation or other asymmetry
      - Constant and dynamic error introduced by preceding network elements
      - Quality of time and frequency recovery of PTP client algorithm
        - PTP slave algorithm may afford some reduction in dynamic time error
    - Outgoing PTP timestamps depend on accuracy of internal time recovery
    - PTP timestamps have similar sources of Time Error as with GM clocks
    - 1PPS may have different Time Error from packet time, as in GM clocks

Testing Boundary Clocks

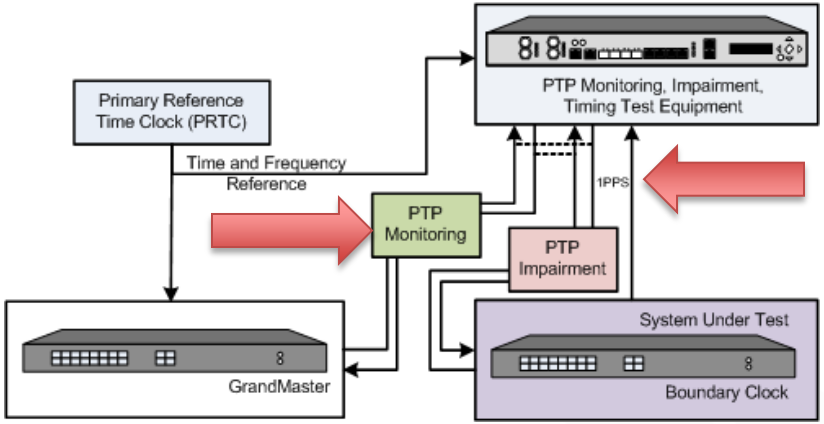
- Boundary Clocks
  - Provide PTP services at network junctions with, possibly, multiple master ports to supply downstream clocks from one slave port
  - Comparatively new devices and industry is still learning
  - Boundary clocks must fit into existing network topologies
- Testing Challenges
  - Boundary Clocks introduce non-linear timing errors whose effects are analogous to time error and PDV produced by busy switches
  - Boundary Clocks may have 1PPS outputs to test the “slave” side of BC but that does not address the master port
- Methods for accurately identifying and analyzing the timing impairments introduced by a boundary clock are maturing

Testing On-path Support (G.8273 Annex A&B)



- BC provides a 1PPS (& opt. frequency) output to verify slave clock recovery performance
- The *PTP Impairment* function introduces impairments in a controlled manner to provide suitable “stress” conditions
- Difference between time at PTP Monitoring points on either side of the BC quantifies the time-error generated by the SUT
- Synchronization error introduced by SUT is passed downstream to slave

Boundary Clocks – 1PPS vs. PTP TE



- Boundary Clocks may be equipped with 1PPS interfaces, offering test options

- 1PPS from the BC should be synchronous with the timestamps
  - Test equipment measures Time Error of both PTP sync/follow-up packets and 1PPS at the same time

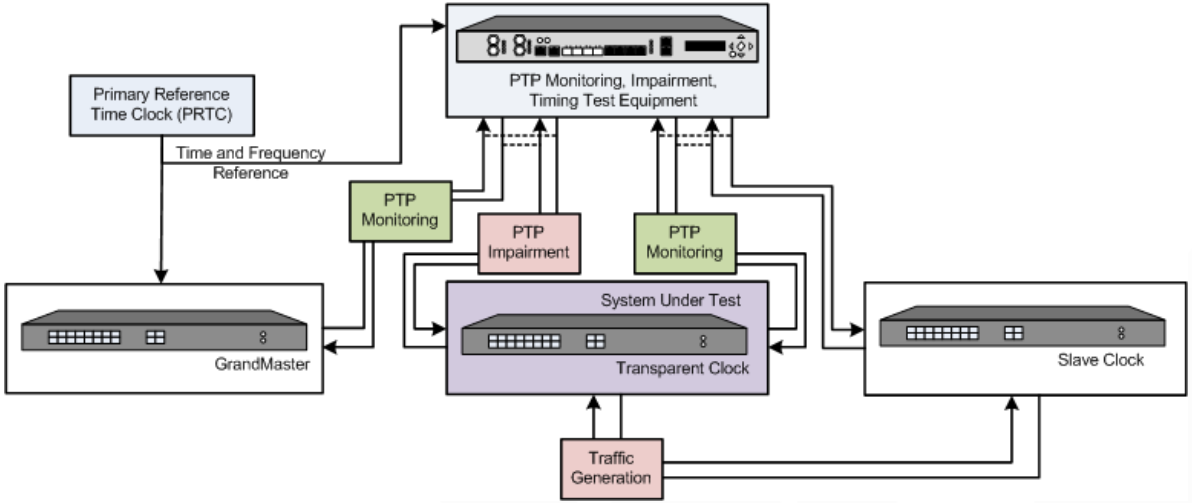
Time Error: Transparent Clocks

- Transparent Clock
  - Passes through Time Error of incoming PTP packets – does not correct time error of incoming packets
  - Adds additional Time Error quantity equivalent to the inaccuracy of the Correction Field
    - PDV or delays introduced by the TC are to be reduced by the Correction Field
    - Correction Field accuracy of real devices varies dramatically
    - Target of 50ns can be difficult to meet and verify
    - Excessive delays, or delays greater than the time interval between PTP packets can cause problems with recovery at the slave end regardless of accuracy of correction field
  - C37 238 defines limit of 50ns of TE for Transparent Clock

Testing Transparent Clocks

- Transparent Clocks
  - Endeavor to reduce the effect of PDV by informing downstream devices of their delays using the correction field (CF)
  - Comparatively new devices and industry is still learning
  - Transparent clocks must fit into existing network topologies
- Testing Challenges
  - Transparent Clocks add noise in their correction field values that may be non-linear with respect to the actual PDV they introduce
  - This noise may be greater in quantity than the uncorrected PDV
- Methods for accurately identifying and analyzing the impairments introduced by a transparent clock are maturing

Testing On-path Support (G.8273 Annex A&B)



- G.8273 On-path Support test guidance can be adapted to measure Transparent Clock
- The *PTP Impairment* function introduces impairments in a controlled manner to provide suitable “stress” conditions
- TC’s residence time of a PTP packet is precisely measured between the PTP Monitoring points, and subtracted from the Correction Field value to derive the CF accuracy
- TC’s Correction Field Accuracy is a direct indicator of effectiveness of On-path Support

BCs and TCs– Not Ordinary Switches

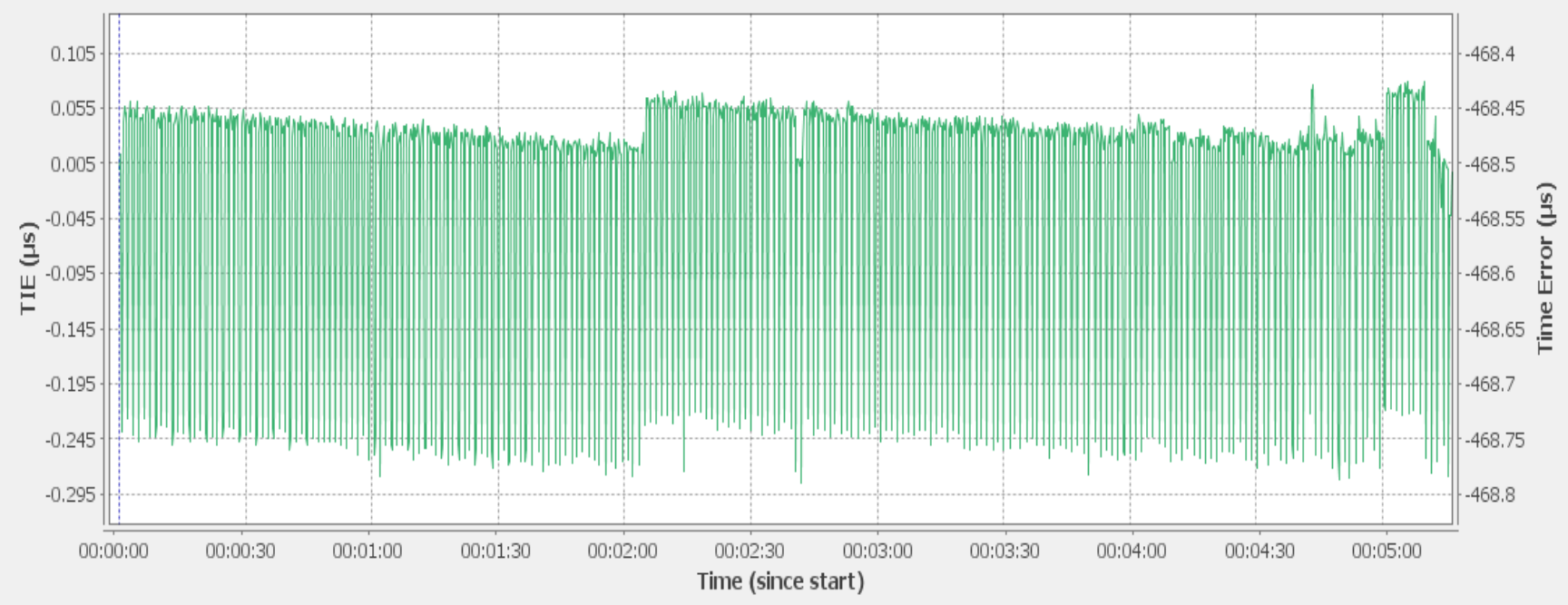
- Real-world testing reveals surprising results: Boundary and transparent clocks ***do*** introduce significant impairments
  - There are sources of time error impairment (constant and dynamic) caused by a boundary or transparent clock that must be evaluated
  - Impact of a boundary clock on frequency recovery may be comparable to that of an ordinary switch with no on-path support (TC under study)
- Methods of testing that consider **both** constant and dynamic impairments are required for validating time/phase transfer

Examples of BC and TC Impairment

- Shown are data from real-world equipment
  - BCs shown are engineering prototypes from one vendor
    - The time error represented here indicates the error in the master port's sync and follow-up timestamps
    - Changes in this impairment were observed when the conditions changed
  - TC shown is a production switch from a different vendor
    - The time error represented here indicates the difference between the origin time-stamp and the actual measured arrival time of the packet, approx. uncorrected PDV
    - Also shown is the correction field accuracy measurement. This is the effective corrected PDV seen by downstream neighbors

Boundary Clock Impairment – BC #1

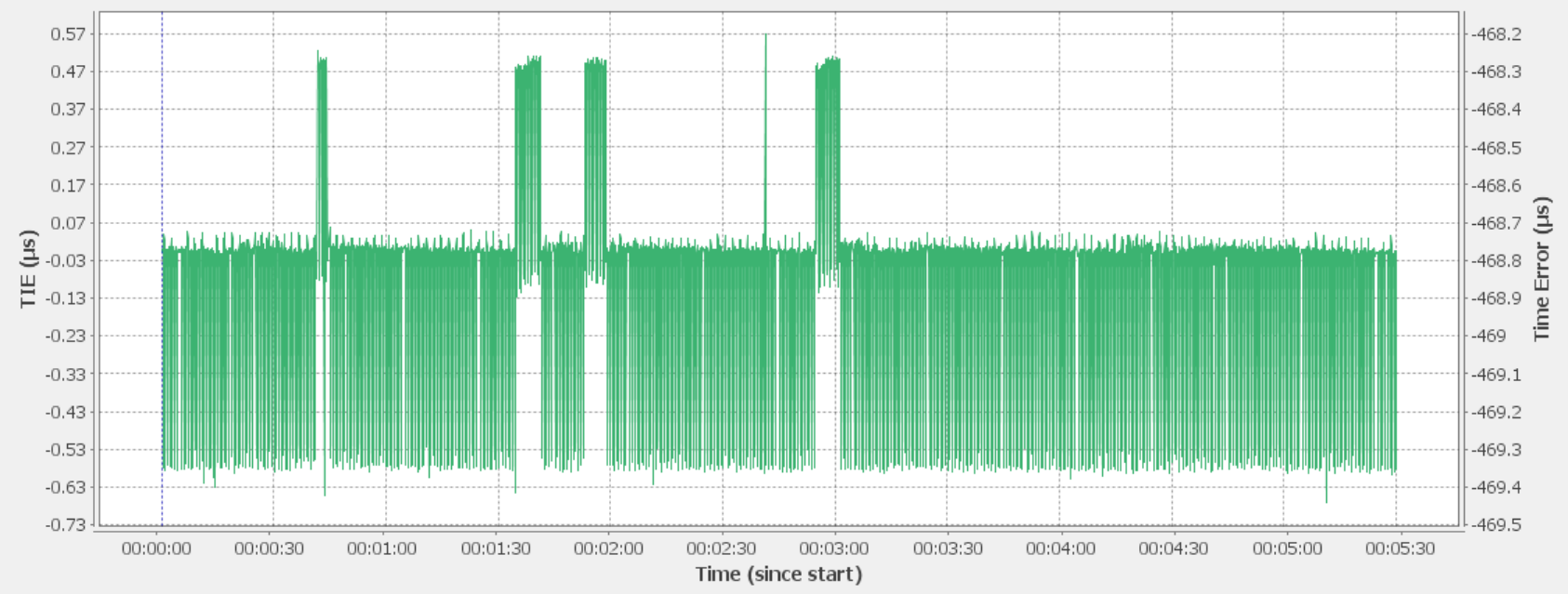
No background traffic, no impairments



- Grand Master sync rate **4pps**
- Boundary clock master-port sync rate **16pps**
- Substantial time error observed during 5-minute window

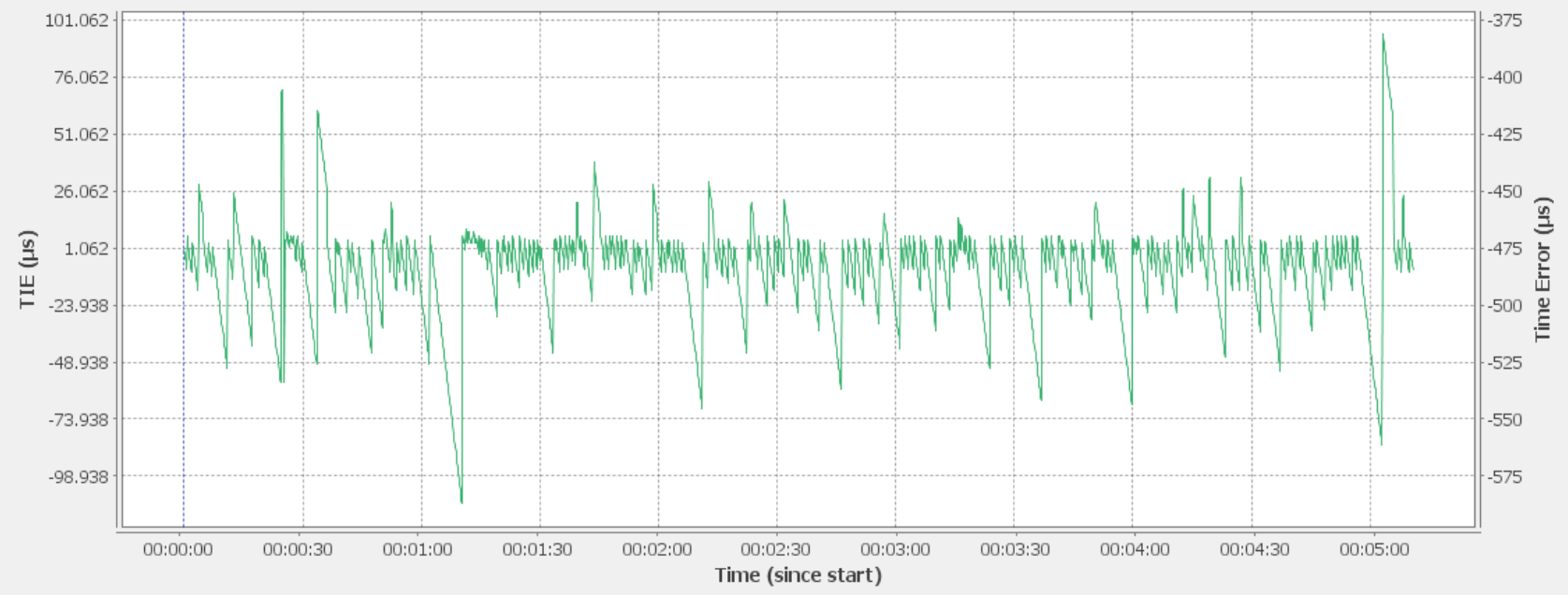
Boundary Clock Impairment – BC #1

No background traffic, no impairments



- Grand Master sync rate **8pps**
- Boundary Clock master-port sync rate **8pps**
- Dramatic change in behavior compared to other sync rate

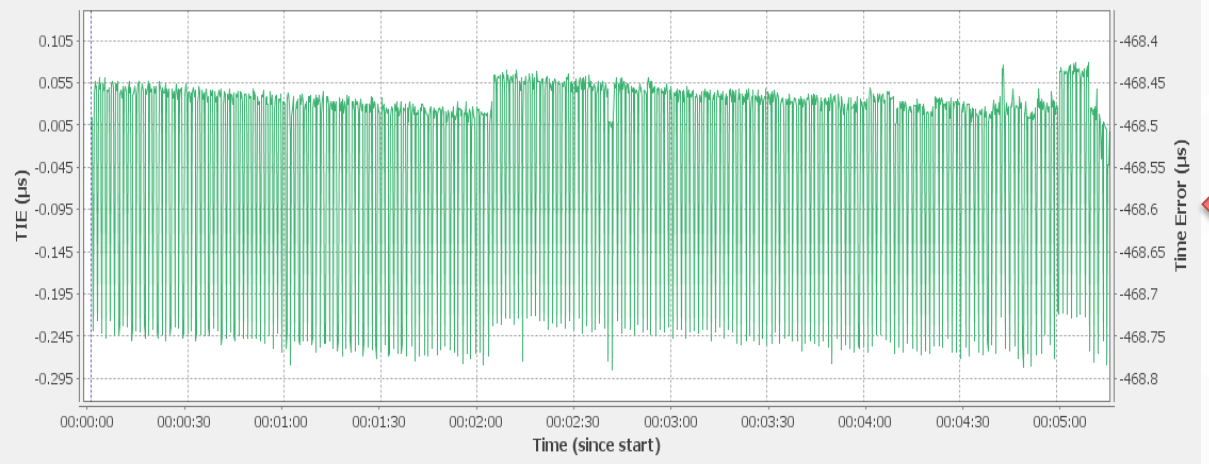
Boundary Clock Impairment – BC #2
no background traffic, no impairments



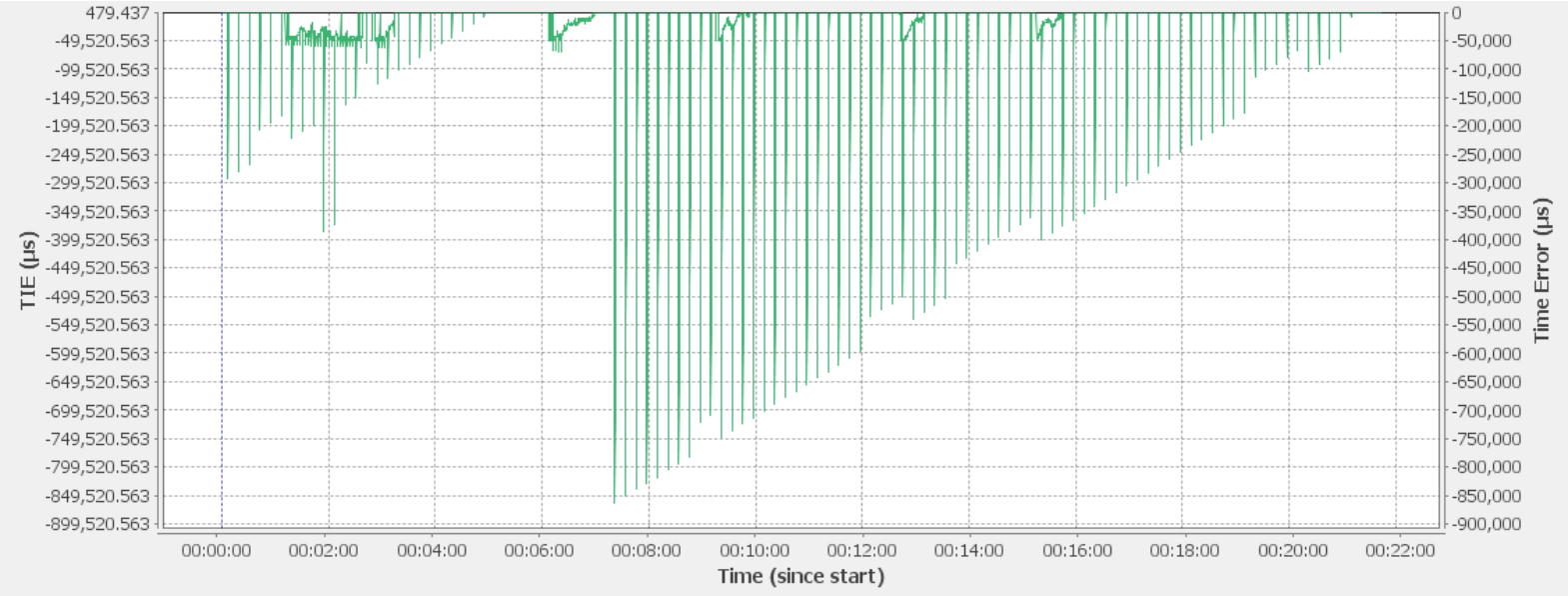
- Grand Master sync rate **8pps**
- Boundary Clock master-port sync rate **8pps**
- A different device has dramatically different results

Boundary Clock Tests: Observations

- Around 50% of 1μs TE budget (static error) is contributed by one switch
- Dynamic error (PDV-like effect) very substantial, will give rise to frequency synchronization error at slave (wander)
- More thorough testing and defined standards are warranted

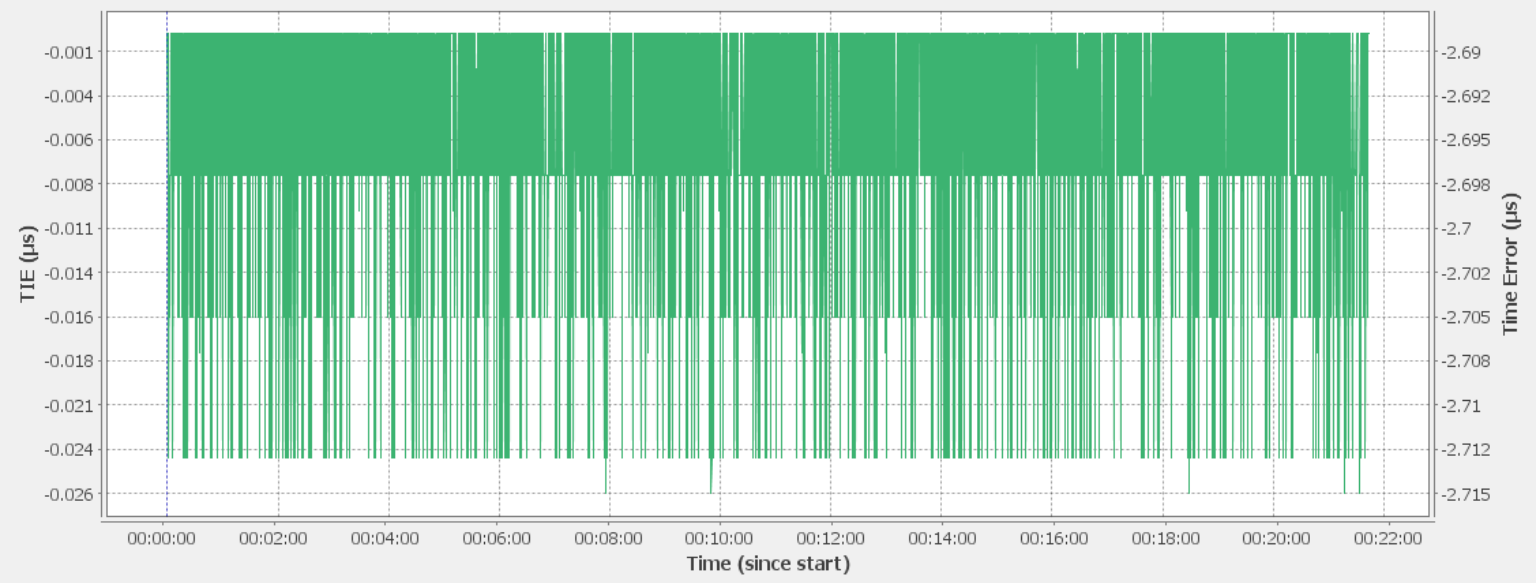


Transparent Clock Behavior



- Graph shows the “raw” delay for sync packets through the TC
- Packet delays of ~900ms were observed (even with no load)
- Grand Master sync rate **4pps**

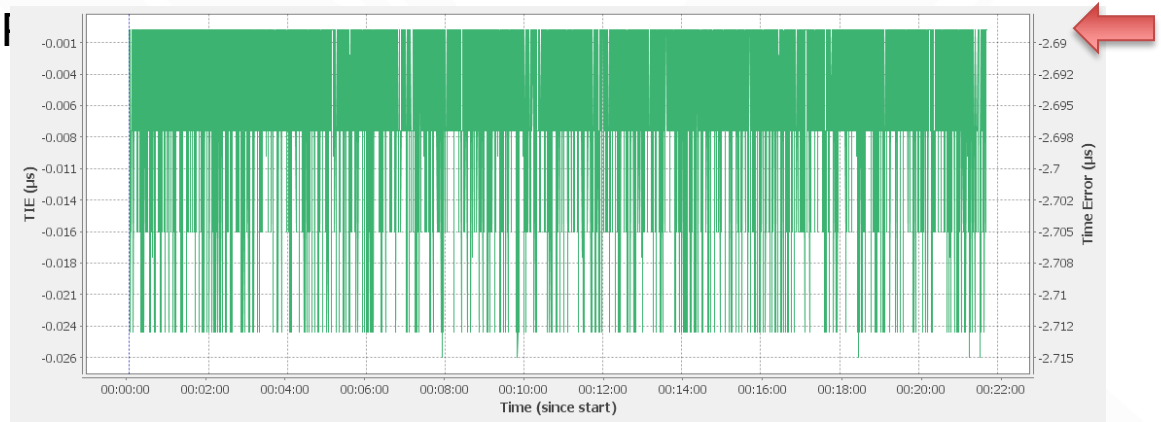
Transparent Clock Behavior



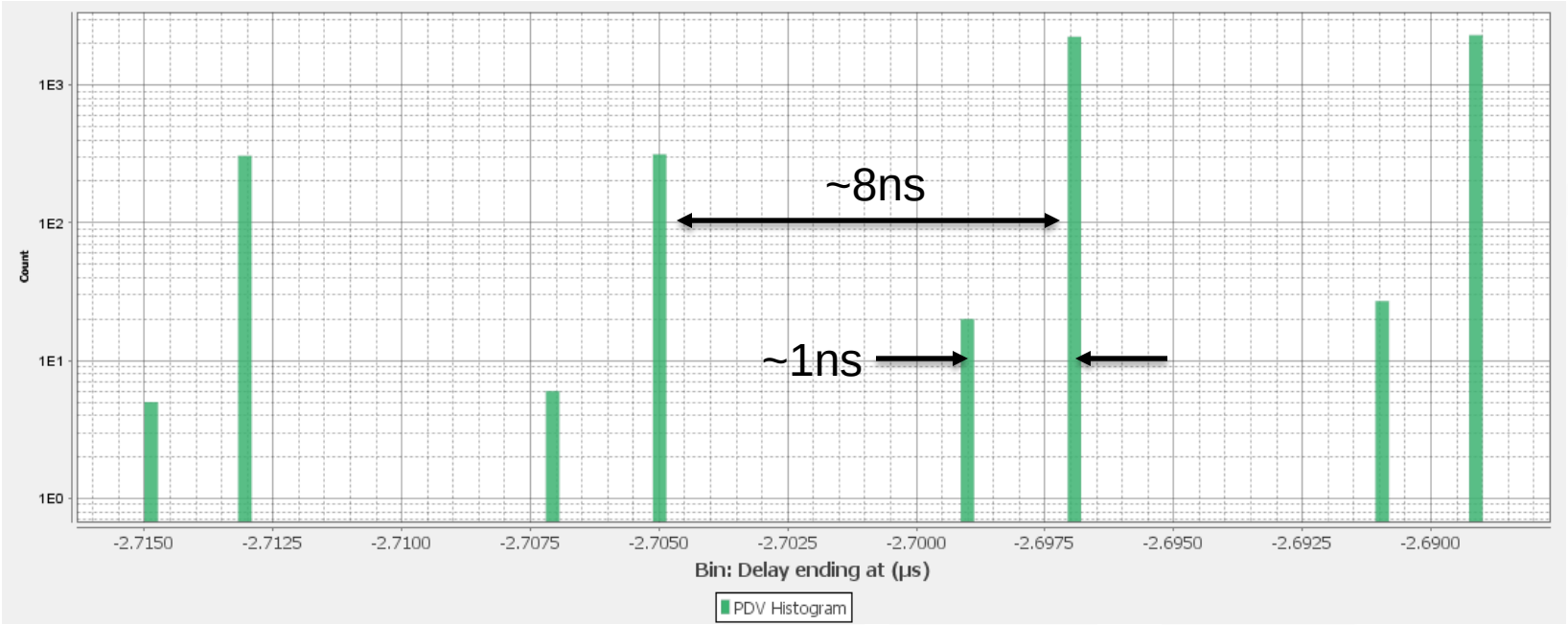
- Graph shows the corrected delay for the sync packets
- Packet delay variation reduced to ~24ns; delay error to ~2.7µs
- TC correction field vs. timing granularity of 8ns is visible
- Note: this behavior was observed to be load independent

Transparent Clock Tests: Observations

- TC on-path support effectively reduced PDV (dynamic component) to 24ns
  - Leaves room for 26ns of static error
- Static Time Error is ~ 2.7μs, >50x the limit
- Excessive delay likely to lead to slave synchronization issues
  - Up to 4x the 0.25 second packet interval
  - Contributes to low FI

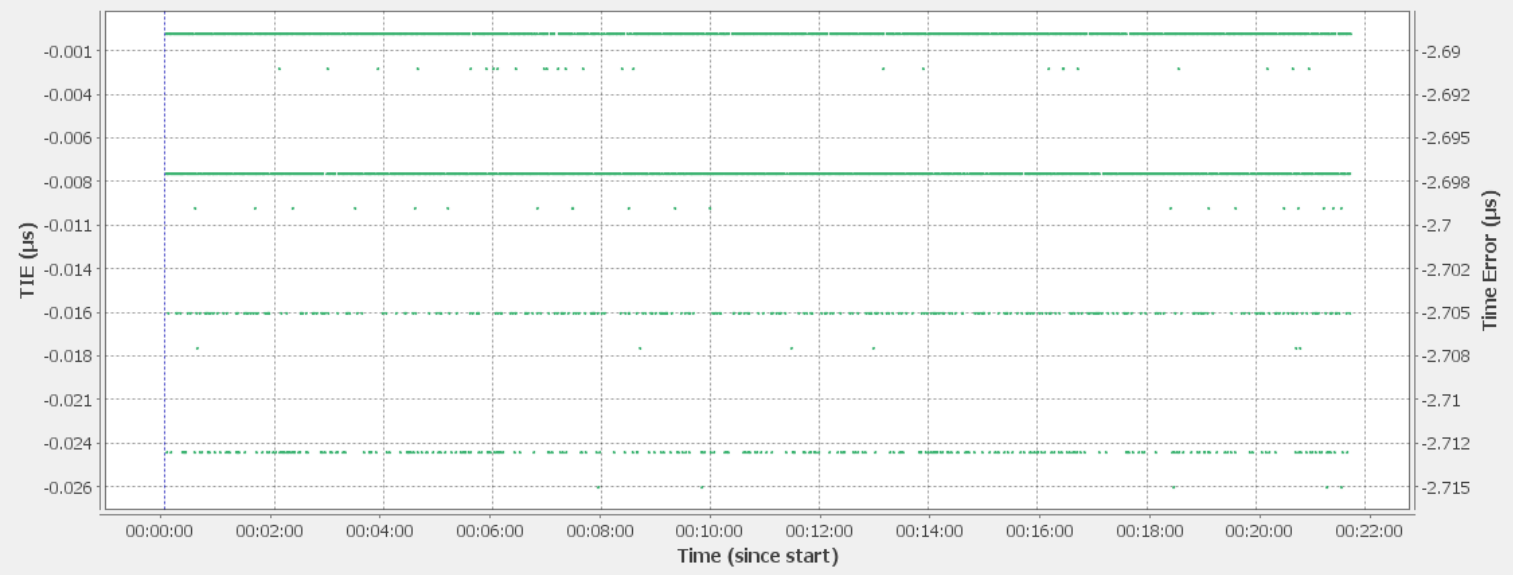


Measuring instrument Granularity



- Histogram view shows the ~8ns granularity of the TC and the ~1ns granularity of the measuring instrument
- Without this granularity, the discrete nature of TC correction error would not be visible

Measuring instrument Granularity



- The TC correction quantization is ~8ns
- Observation of this granularity requires test device to measure with a precision of much better than ~4ns
- The measurement granularity of the test equipment is seen to be ~1ns

Concluding Remarks

- Measuring time error (constant and dynamic) increasing in importance
  - “Frequency” metrics (PDV) necessary but not sufficient
- Boundary clocks (and transparent clocks) are not perfect
  - Cannot chain them indefinitely
  - Effectively introduce static as well as PDV-like (dynamic) timing impairments (time error)
- Reason for impairments may be implementation dependent
  - BCs measured were affected by sync rates and traffic loads
- G.8273 Annex A and Annex B address GM/BC/TC testing
- Testing during equipment development phase is very helpful

Thank You!
Questions?

Back-up Slides

Boundary Clock Challenges
Inaccurate Clocks

- Boundary Clocks Introduce Impairments
  - Internal Clock
    - An internal clock is derived from the PTP on the slave port of the BC in the usual manner and this local clock is used to create time-stamps on outgoing PTP traffic
    - Inaccuracy in this clock creates impairment:
      - Inaccurate time-stamps going out the master port; *time-stamp does not accurately indicate the true real time*
    - **any errors result directly in inaccuracy in the downstream clock recovery**
  - System (PHY) clock
    - The system clock or PHY clock may be asynchronous with respect to this internal PTP-derived clock
      - Any difference in these two clocks results directly in inaccurate time-stamps**, even if the PTP internal clock is perfect**

Boundary Clock Challenges Not Ordinary Switches

- Many boundary clocks are multi-function devices with many features not related to timing that compete for resources with PTP
  - L2 features such as spanning tree, VPNs, redundancy, VLANs, etc.
  - QoS – L2 & L3, different egress and ingress, marking, priority, etc.
  - Routing, Switch Virtual Interfaces, Routing Protocols, VRFs, MPLS
- Architecture of these devices may not be ideal for PTP
  - Designed primarily for fast switching of packets from port to port
  - Limited emphasis on speed, latency, etc. of CPU-generated or control-plane traffic
- These caveats of Boundary Clocks are important to characterize
  - They may not typically perform like a standard L2 switch with respect to PDV
  - They may have significant impact on the performance of PTP networks
- *A boundary clock cannot simply be treated as if it were an ordinary switch for testing purposes*

Testing Questions Remain

- Important questions remain regarding BC/TC testing
  - What limits or metrics are applicable for impairment introduced by a boundary clock as in Test Scenario #1?
    - TIE / PDV? Maximum Time Error? What limit is to be expected?
    - Will require both: *constant time error* (“static”), as well as TIE/PDV (“dynamic”)
  - What PDV impairment profiles apply to test with impairments before and after the Boundary Clock as in Test Scenario #2?
    - Does some model apply which emulates *N* number of Boundary Clocks, or networks combining Boundary Clocks with ordinary switches?
  - What is the precision/accuracy required in the test equipment?
    - Rule-of-thumb: at least one order of magnitude better than the same function in the DUT (e.g. time-stamping)
    - Test signal generation (e.g. introduction of wander):

Testing Challenges
Boundary Clock as Slave or Master

- Testing Boundary Clock as a slave or ordinary clock
  - Many Boundary Clocks do not have recovered clock interfaces to measure
  - The standard G.8261 tests are performed without regard for the Boundary Clock's master port behavior, therefore do not address the purpose of the boundary clock
  - This test does not address the time impairment introduced by circuitry between the boundary clock's slave and master ports
- Testing Boundary Clocks as a master clock
  - The standard G.8261 tests are performed with PDV impairment is added between Boundary Clock and slave. Slave's recovered clock interface is evaluated against the standard MTIE/TDEV masks
  - This test does not address the ability of the Boundary Clock to recover an accurate clock in the presence of time error between the BC and the GM
  - The Boundary Clock is not being measured directly; the result is dependent on the performance of the slave device

Boundary/Transparent Clock Testing
Suggested Best Practices

- Monitoring/measuring time error on both sides of a boundary/transparent clock
  - Comparison between input and output reveals the static and dynamic impact of the device and we can verify whether it is affected by
    - Background traffic, incoming and outgoing sync packet interval, QoS, routing, etc
- Impairment on both sides of a boundary/transparent clock
  - Impairment is added between the GM Clock and BC/TC, and between the BC/TC and slave clock, simultaneously; recovered clock at remote slave is measured
    - Profiles need to be developed
- Measure ToD error and phase (1PPS) error introduced by boundary clocks
  - Monitor and measure timestamp accuracy of sync, follow-up packets from master port of boundary clock and measure phase offset of 1PPS between GM Clock and Slave with boundary clock in between