



## Moving Towards Higher Performance Boundary Clocks

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# Investigation Topics

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1. HP-BC Optical Asymmetry Investigation
2. HP-BC Chain Time Error Accumulation
3. HP-BC Node and Link Loss/Recovery Operation

# Bi-Directional Optical Asymmetry Investigation

Objective: observe the time asymmetry introduced over the fiber optic path.

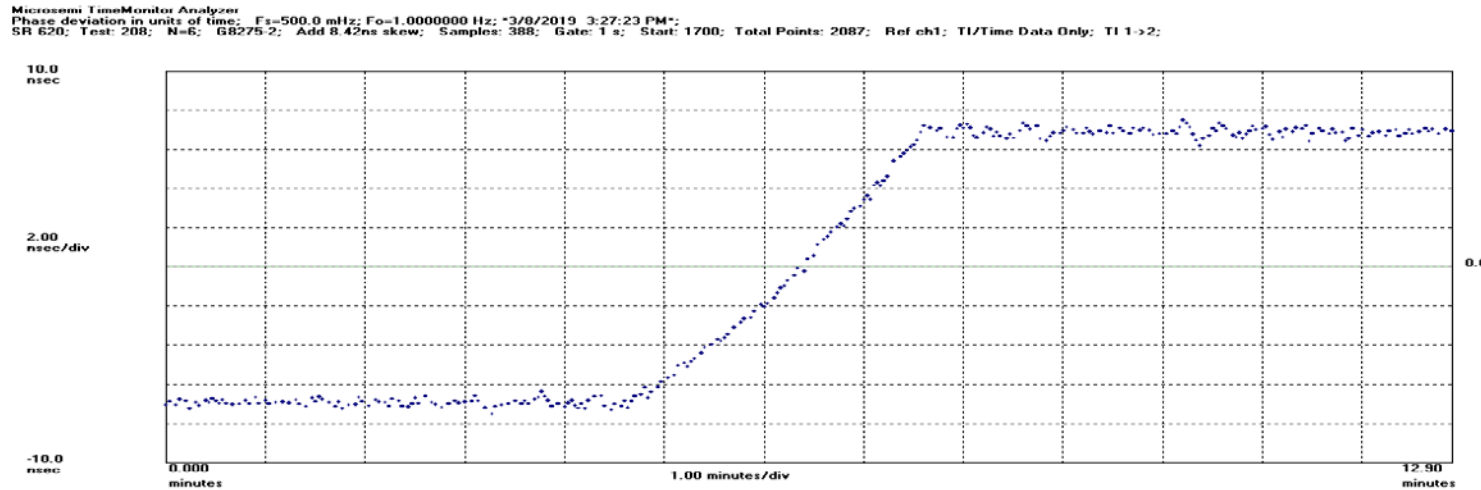
The path is supported with:

- 1) 83.633 km of single mode Corning G.652.D Fiber
- 2) Bi-Directional SFPs Investigated
  - Case 1: 1605/1615 nm Bi-Directional SFPs
  - Case 2: 1290/1350 nm Bi-Directional SFPs

The test sequence is:

- 1) Start system with the PRTC GM operating with:
  - Case 1: 1605 transmit SFP.
  - Case 2: 1290 transmit SFP.
- 2) Collected data for nominally 15 minutes
- 3) Disconnect Fiber and SFPs and swap the SFPs so that the GM now transmits longer wavelength.

# Case 1:1605/1615nm Test



The time error average before and after the switch is +/- 6.92ns.

The total excursion of 13.84ns is the measured delay difference.

What is the simple first order predicted asymmetry?

The dispersion effect at 1600nm is nominally 17ps/km/nm.

$$17e-12 * 83.633 * 10 = 14.22ns$$

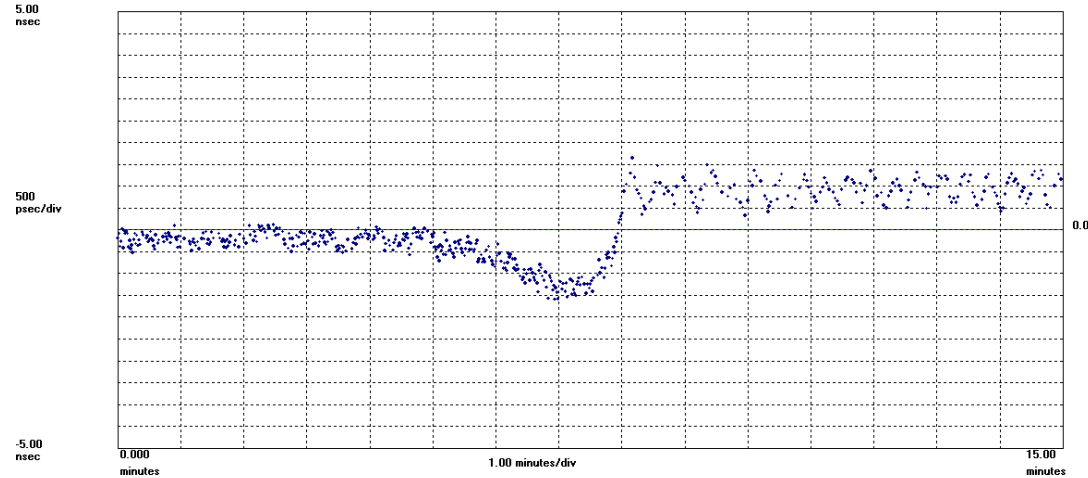
The error using this simple first order correction term is:

$$0.5(14.22-13.84) = 0.19ns.$$

The error is less than 1ns with an application of this compensation term.

# Case 2:1290/1350nm Test

Microsemi TimeMonitor Analyzer  
Phase deviation in units of time: F=777.2 MHz; Fo=1.0000000 Hz; \*3/9/2019 11:44:38 AM\*  
SR 620; Test: 205; N=1; 8275.2 64Hz; 0 Skew Correct; Samples: 701; Gate: 1 s; Start: 789; Total Points: 1489; Ref ch1; T1/Time Data Only; T1 1->2;  
80km High Accuracy BC



The time error average before and after the switch is +/- 0.56ns.

The total excursion of 1.12ns is the measured delay difference.

What is the simple first order predicted asymmetry?

The dispersion effect at 1300nm is nominally +/-1ps/km/nm (near zero dispersion point for the fiber).

For the sake of simplicity, we'll assume the Bi-Di SFP is close to 0 dispersion effect :

$$0 * 83.644 * 60 = \sim 0\text{ns}$$

The error using this simple first order correction term is:

$$0.5(1.12 - 0) = 0.56\text{ns}$$

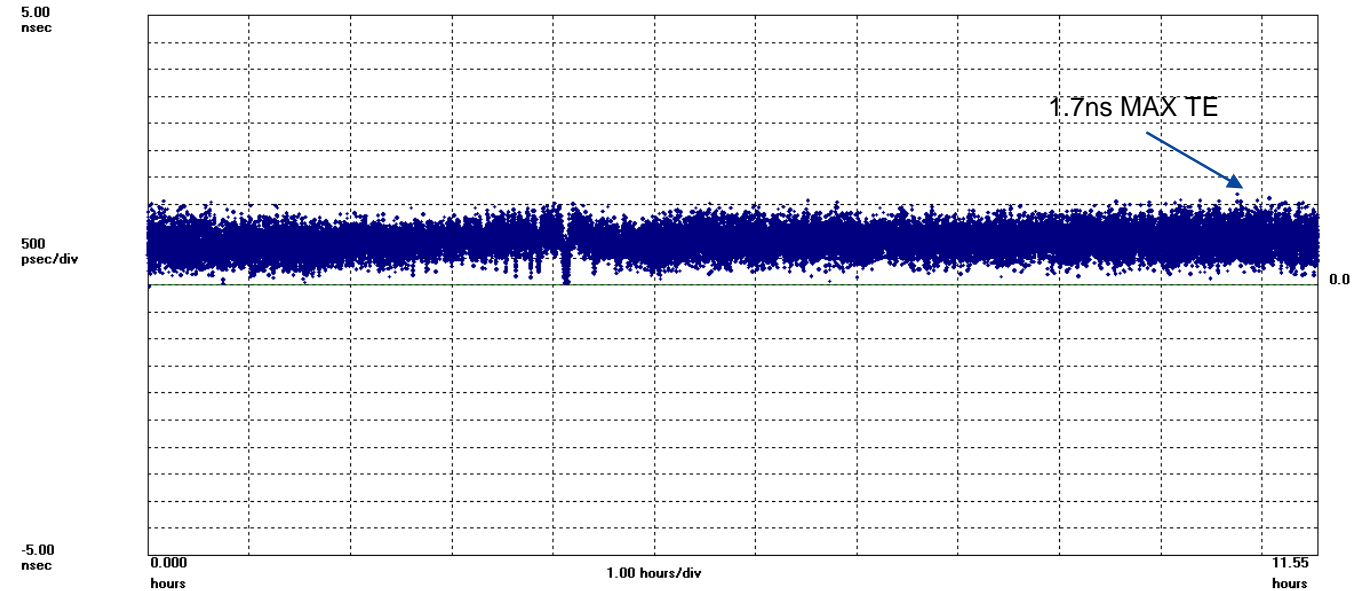
The error is less than 1ns with an application of this compensation term.

# Case 1: 85km 1600nm with Compensation

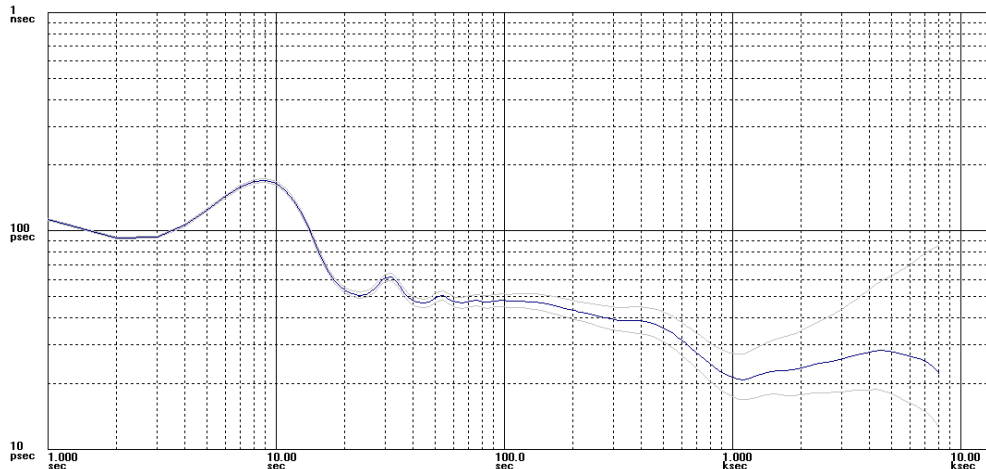
## Observations:

- Time Error graph include 0.1Hz proposed filter
- Measured MAX|TE| = 1.7ns well within 5ns Class D requirement.
- This test includes both the high accuracy BC and 85km of fiber optic link which is not required to pass Class D!
- TDEV stability characteristic is shown below. Floor is 30ps.

Microsemi TimeMonitor Analyzer  
Phase deviation in units of time: Fs=1.000 Hz; Fo=1.0000000 Hz; 2019/03/21; 20:07:37  
SR 620; Test: 265; N=6; G8275-2; Add 8.42ns skew; Samples: 41571; Gate: 1 s; Start: 1000; Total Points: 42570; Ref ch1: T1/Time Data Only; T1 1->2;  
EXP\_6 Master to EXP\_6 Client



Microsemi TimeMonitor Analyzer  
TDEV: Fo=1.000 Hz; Fs=1.000 Hz; Cl=0.954; FPM: 2019/03/21; 20:07:37  
SR 620; Test: 265; N=6; G8275-2; Add 8.42ns skew; Samples: 41571; Gate: 1 s; Start: 1000; Total Points: 42570; Ref ch1: T1/Time Data Only; T1 1->2;  
EXP\_6 Master to EXP\_6 Client



# Chain of Boundary Clock Investigation

This test is design to observe the time error accumulation over a chain of High Performance Boundary Clocks:

The path is supported with:

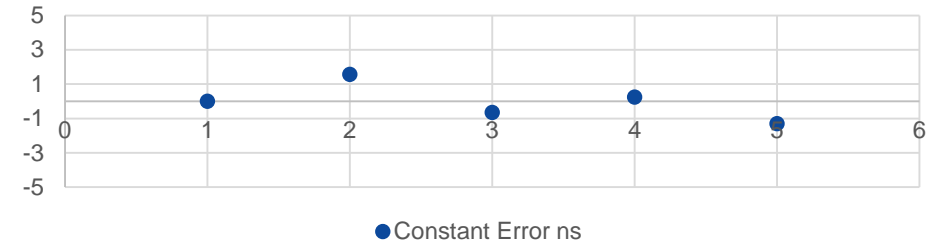
- High Performance Boundary Clock key parameters:
  - OCXO (SC cut)
  - 1ns Multiphase Clock Sampling Technique
  - G8275.1(16Hz) and G8275.2(64 Hz) (With OCXO results are essentially equivalent)
  - 33ps controlled phase stepper based synthesizer
- Path originates with a PRTC level GM clock
  - GM clocks has same 1ns Multiphase Clock Sampling Time Stamper.
  - GM is driven by GNSS simulated ideal signal that is locked to the house timescale.

# Chain of High Performance Boundary Clocks Overall Performance

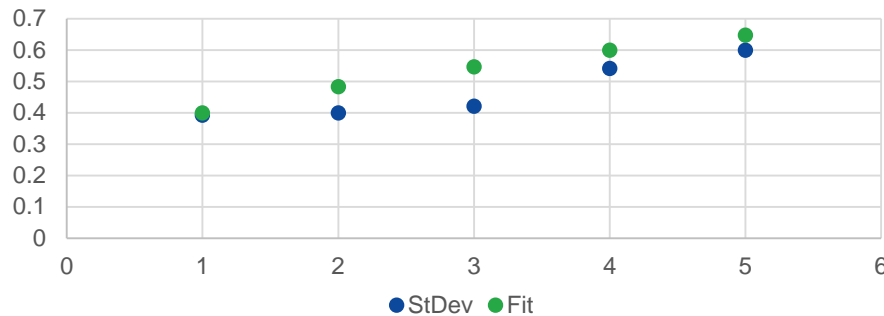
## Observations:

- No appreciable growth in constant time error.
- Dynamic noise accumulation shows modest growth well bounded by  $\sqrt{N}$  bound.
- Class D performance maintained over 6 nodes.

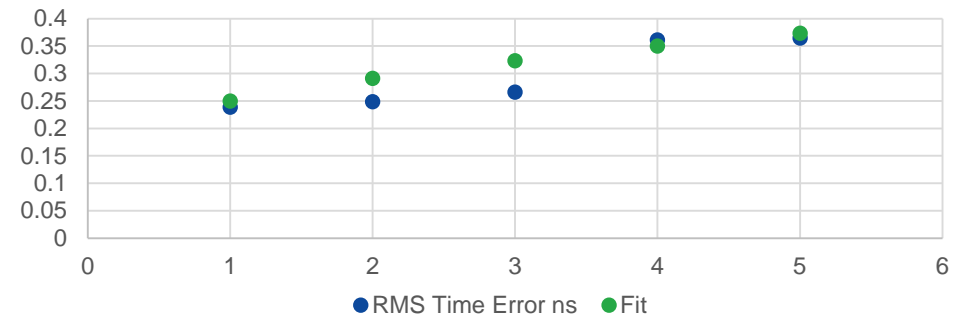
### Constant Time Error Accumulation



### Peak Stdev Noise Accumulation Fit: $200\text{ps} + 200\text{ps} \cdot \sqrt{N}$



### Peak Tdev Noise Accumulation Fit: $100\text{ps} + 150\text{ps} \cdot \sqrt{N}$



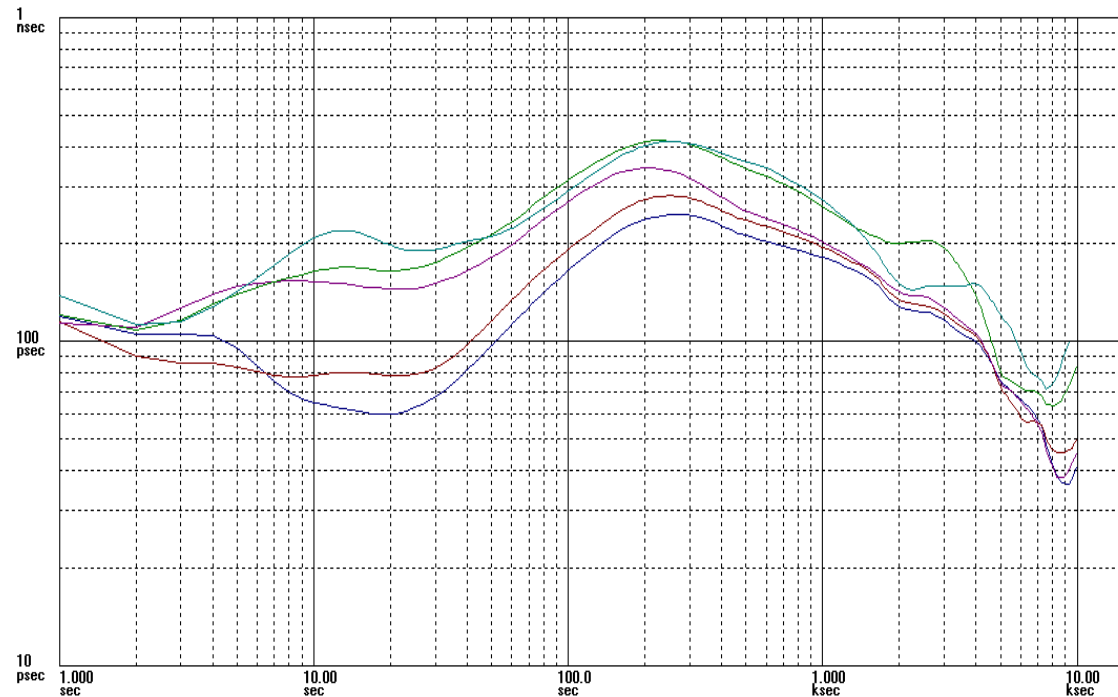


# Chain of High Performance Boundary Clocks TDEV Stability

Observations:

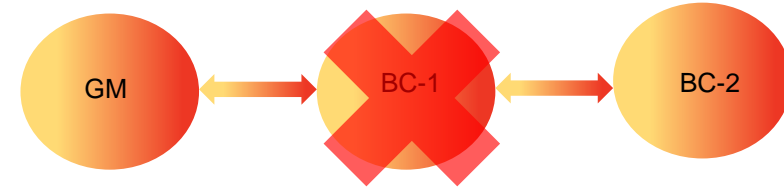
- Tracking Loop Steady State Bandwidth is observed in the TAU associated with the peak.
- The growth in the peak is well behaved ( $\sqrt{N}$ )

Microsemi TimeMonitor Analyzer  
TDEV; Fo=1.000 Hz; Fs=1.000 Hz; CI=0.954; FPM; 2019/03/12; 17:33:11



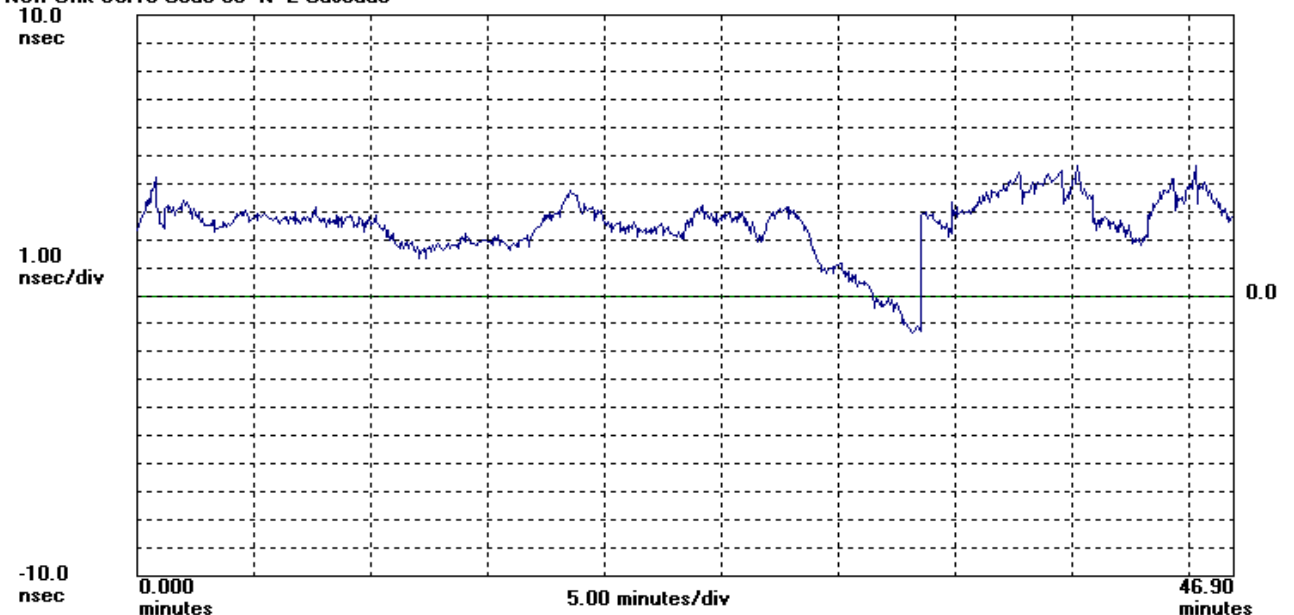
# Chain of High Performance Boundary Clocks Failure Scenario Loss of Node

- PRTC GM provides a direct fiber connection to BC-1
  - BC-1 provides a direct fiber connection to BC-2.
- Procedure:
- Warmup for nominally 30 minutes
  - Remove power for 30 seconds from BC-1 and then restored.



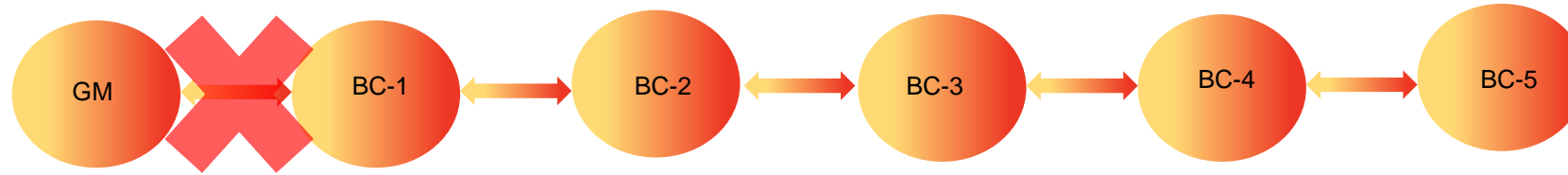
The timing performance of BC-2 is observed during this failure scenario. The external time error graph starts about ten minutes prior to the power cycle fault introduced at BC-1. Keep in mind that this is the output of the second boundary clock in the chain so strictly speaking the Class D limits do not directly apply. Also the constant time error is not corrected in this test. The high performance BC is able to maintain these accuracy limits in this test case.

Microsemi TimeMonitor Analyzer  
Phase deviation in units of time; Fs=500.0 mHz; Fo=1.0000000 Hz; \*9/25/2018 7:30:03 PM\*;  
SR 620; Test: 823; CLASS\_C\_D Demo; Samples: 1408; Gate: 2 s; Ref ch1; TI/Time Data Only; TI 1->2;  
New Unit Servo Code 35 N=2 Cascade

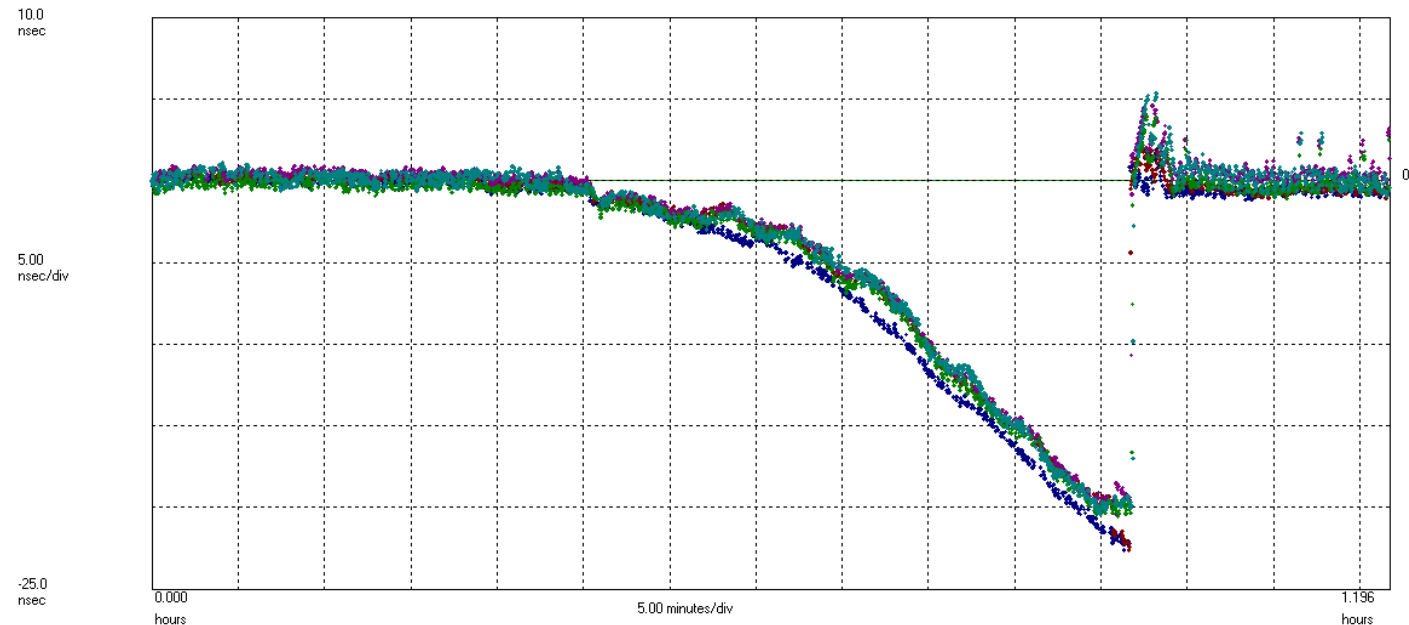


# Chain of High Performance Boundary Clocks Failure Scenario Loss of Link

In this test the fiber link is disconnected to BC-2 through BC-6 and then reattached nominally 30 minutes later.



Microsemi TimeMonitor Analyzer  
Phase deviation in units of time; F<sub>s</sub>=999.1 mHz; F<sub>o</sub>=1.0000000 Hz; 2019/03/22; 16:31:18



# Summary

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1. High Performance Boundary Clock Technology using current technology performance was presented.
2. Fiber optical path asymmetry can be addressed well within Class D proposed requirements
3. Operational Issues such as Fiber and Node Loss are addressable with suitable holdover oscillators.