Test Strategy for eSYNCE with Extended ESMC

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Agenda

- G.8264 (Extended ESMC - eESMC)
- G.8262 (EEC)
- G.8262.1 (Enhanced EEC - eEEC)
- Compliance Tests
- Sample outputs

G.8264 (Extended ESMC)

- The ESMC protocol is specified in the G.8264 standard, had been updated to add a new extended QL TLV.
- As part of the ESMC protocol, the quality level (QL) of timing signals is distributed via SSMs.
- This new feature is an extension to the G.8264 standard, in which a new extended QL TLV is described.
- The extended QL allows more precise quality discrimination for very accurate clocks and is a prerequisite for enhanced SyncE (eSyncE) .

QL TLV

Octet number	Size/bits	Field
1	8 bits	Type: 0x01
2-3	16 bits	Length: 00-04
4	bits 7:4 (Note)	0x0 (unused)
	bits 3:0	SSM code
NOTE – Bit 7 of octet 4 is the most significant bit. The least significant nibble, bit 3 to bit 0 (bits 3:0) contains the four-bit SSM code.		

Extended QL TLV

Octet number	Size/bits	Field
1	8 bits	Type: 0x02
2-3	16 bits	Length: 0x0014
4	8 bits	Enhanced SSM code (see Table 11-6)
5-12	64 bits	SyncE clockIdentity of the originator of the extended QL TLV (Note 1)
13	8 bits	Flag (Note 2)
14	8 bits	Number of cascaded eEECs from the nearest SSU/PRC
15	8 bits	Number of cascaded EECs from the nearest SSU/PRC
16-20	40 bits	Reserved for future use

Extended QL TLV

- A new TLV is added to SSM packets containing:
  - A second SSM code
  - Originator clock-id
  - Number of cascaded eEECs from nearest SSU/PRC.
  - Number of cascaded EECs from nearest SSU/PRC.
  - Flags containing:
    - Bit 0: means mixed EEC/eEEC (Are all the steps in the chain eSyncE?)
      - If 0: its not mixed , all clocks in chain are eEEC.
      - If 1: its mixed (i.e., at least one the clocks is not eEEC)
    - Bit 1: mean partial chain (Was the TLV generated in the middle of the chain?)
      - If 0: TLV not generated in middle of the chain and count of EEC/eEEC is complete
      - If 1: TLV has been generated in middle of the chain and count of EEC/eEEC is not complete.

New SSM Codes

Table 11-8 – SSM codes and enhanced SSM codes for SyncE in option 2 networks

Clock	Quality level	SSM code	Enhanced SSM code
PRS	QL-PRS	0001	0xFF
(Note)	QL-STU	0000	0xFF
ST2	QL-ST2	0111	0xFF
TNC	QL-TNC	0100	0xFF
ST3E	QL-ST3E	1101	0xFF
ST3	QL-ST3	1010	0xFF
EEC2	QL-EEC2	1010	0xFF
(Note)	QL-PROV	1110	0xFF
(Note)	QL-DUS	1111	0xFF
PRTC	QL-PRTC	0001	0x20
ePRTC	QL-ePRTC	0001	0x21
eEEC	QL-eEEC	1010	0x22

NOTE – There is no clock that corresponds to this quality level.

Clock ID

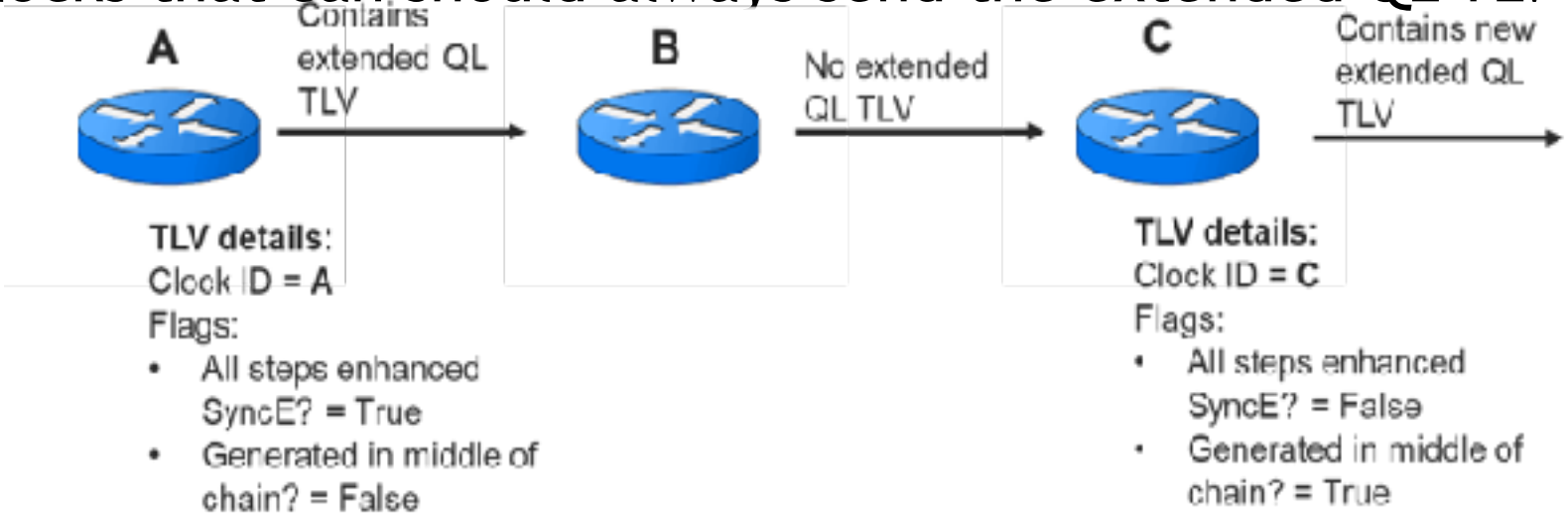
- New to Frequency synchronization.
- The originator of extended QL TLV refers to clock that starts or restarts the counts of cascaded clocks within the extended QL TLV.
- Clock Id will be derived out based on MAC address of the router.
- There is an option to configure the clock-id manually by user.
- Clock-ID should be unique in the given domain.
- Sample Clock ID : 0x405539fffe6a7610

Functional Model

- If the box is eSyncE enabled, we increment both “Number of cascaded” counters.
- If the box is SyncE enabled, we only increment the “Number of cascaded EECs from nearest SSU/PRC ” counter.
- The values to send are set on the ‘send-side’ and therefore the grandmaster will send out value of 1 for both these “Number of cascaded” counter.
- When converting the new QL values in PTP, we use the same conversions as used for the non-enhanced QLs.
- For the rankings, **eEEC > EEC and ePRTC > PRTC > PRC/PRS.**

Interworking Model with legacy

- Boxes must drop any TLVs that they don't recognise.
- The TLV 'flags' are used to inform downstream boxes that this has happened.
- Clocks that can should always send the extended QL TLV



Scenarios

1. **All node support eSyncE with enhanced ESMC**

- Both eEEC and EEC “number of cascaded” counters will be incremented.
  - Ex: If there are 10 nodes in chain, eEEC and EEC cascaded counter will be 10 at the last node output.
- Flag filed bit 0 (is it mixed eEEC and EEC?) will be set to 0
- Flag filed bit 1 (is it partial chain?) will be set to 0

Scenarios

2. One node in middle do NOT support eSyncE but support SyncE with enhanced ESMC

- If there are 10 nodes in the chain and 1 node does not support eSyncE but supports enhances ESMC:
- Only SyncE/EEC cascaded counter will be incremented by node no supporting eSyncE and supporting enhanced ESMC.
  - at the end node eSyncE/eEEC cascaded count will be 9, SyncE/EEC cascaded count will be 10
- At first node both flag field bits will be set to 0.
- The node not supporting eSyncE but supporting enhanced ESMC:
  - Flag field bit 0 will be set to 1 (indicating it is mixed eSyncE and SyncE nodes chain)
  - Flag filed bit 1 will be set to 0 (indicating Extended QL-TLV is not dropped, as SyncE node also supports extended ESMC)

Scenarios

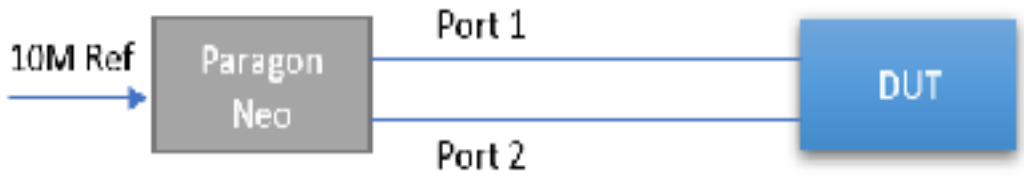
3. One node in middle do not support eSyncE and also do not support enhanced ESMC.

- The node not supporting enhanced ESMC drops QL-TLV received from previous node supporting eSyncE.
- The next node supporting enhanced ESMC starts fresh “cascaded” count (starts with 1).
  - “cascaded” count changes depends on support of SyncE or eSyncE.
- Flag filed bit 0 (is it mixed eSyncE and SyncE?) will be set to 1
- Flag filed bit 1 (is it partial chain?) will be set to 1

eSyncE Compliance Tests

- Frequency Accuracy
- Pull in/Hold in Range
- Noise Generation
- Noise Tolerance
- Noise Transfer
- Transient Response
- Holdover Performance

Sample Test Topology



G.8262 Vs G.8262.1

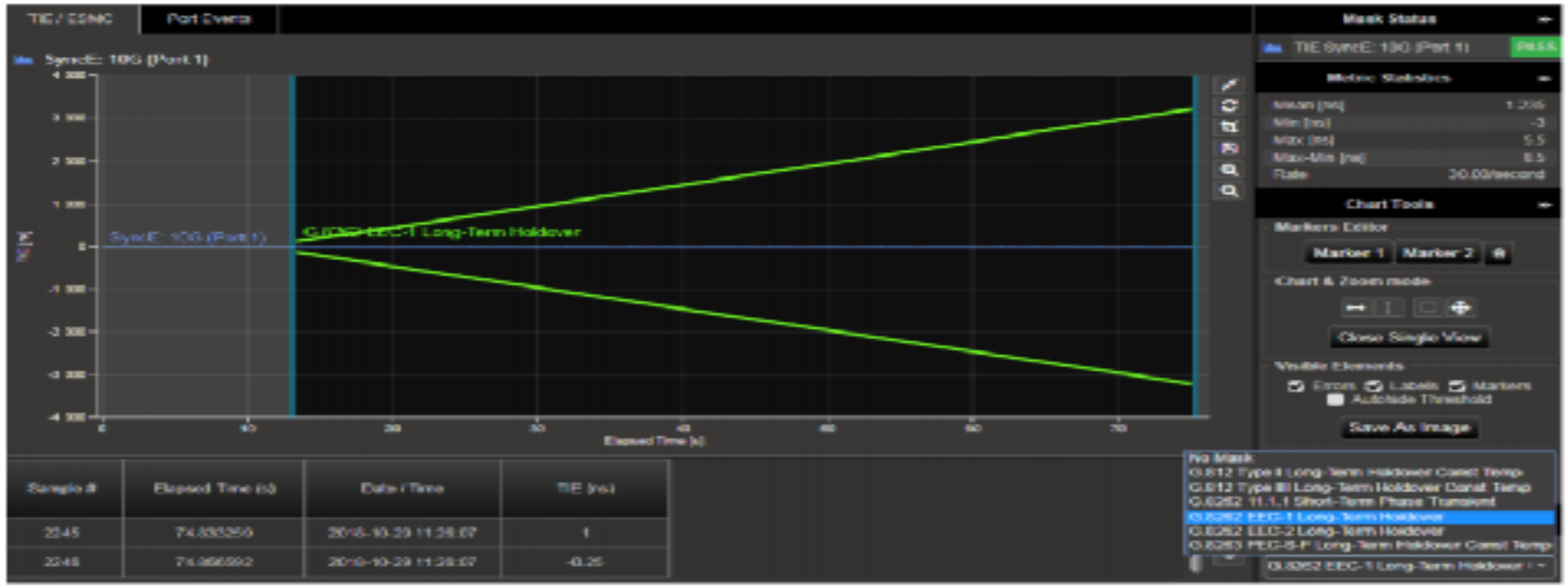
Test Cases	EEC (G.8262)	eEEC (G.8262.1)
Frequency Accuracy	+/-4.6 ppm	+/-4.6 ppm
Pull-in/Hold-in	+/-4.6 ppm	+/-4.6 ppm
Wander Generation	MTIE: 40ns @ 0.1s, rising to 113 ns @1000s TDEV:3.2ns @ 0.1s, rising to 6.4 ns@1000s	MTIE: 7ns @ 0.1s, rising to 25 ns @1000s TDEV:0.64ns @ 0.1s, rising to 1.28 ns@1000s
Wander Tolerance	250ns @ 0.1s, rising to 5000 ns @1000s	Same Value
Jitter Generation	0.5 UI(1G,10G) 1.2 UI(25G Lanes)	Same Value for 1G 10G, 25G -Further Study
Jitter Tolerance	250 ns @10Hz, reducing to 1.5 UI (3.6 UI for 25G Lanes)	Same Value for 1G 10G, 25G -Further Study
Clock Bandwidth	1-10 Hz	1-3 Hz
Transient Response	120 ns at Initial step, then 50 ns/sec (Const Temp.)	10 ns at Initial step, then 10 ns/sec (Const Temp.)
Holdover	120 ns at Initial step, then 50 ns/sec frequency offset, plus 1.16 X 10-4 ns/s2 drift	10 ns at Initial step, then 10 ns/sec frequency offset, plus 1.16 X 10-4 ns/s2 drift

Sample Results

Transient Response :

Sample Results

Holdover Performance :



Thank You !!!